NOVEL REVERSIBLE 16*16 WALLACE TREE MULTIPLIER USING TSG GATES

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ABSTRACT

*In the current era, reversible logic has emerged as a potential computing model as it afford less power consumption which makes it applicable for low power CMOS design, optical computing, quantum computing and nanotechnology. This paper describes about the implementation of reversible logic for ALU operation via TSG gate and compressor. It utilizes a 4*4 reversible gate called TSG gate which can work independently as a reversible full adder, unlike the full adder circuit designed from conventional set of gates such as AND, OR and NOT which are not reversible. A Novel reversible 4:2 compressor is also designed and used to build a novel 16*16 Wallace Tree Multiplier. With the inference of this paper, it is proved that full adder, reversible 4:2 compressor and the multiplier architectures designed using the TSG gate are beneficial than their equivalents available in literature, in terms of number of garbage outputs and reversible gates. Thus, this paper provides a foundation to build more complicated circuits without much power dissipation.*

Keywords: Quantum Computing, Reversible Logic, Reversible Gates, TSG Gate, Wallace Tree Multiplier.

I. INTRODUCTION

This section provides contextual meaning of reversible logic and purpose behind it.

1.1 Descriptions

With the increasing complexity of CMOS VLSI design, power dissipation has become the main area of concern in VLSI design. In 1961, it has been demonstrated by the researcher called Landauer that circuits and systems built using irreversible gates will result in power consumption and energy dissipation due to information loss in the form of bits [1]. It is proved that the loss of one bit of information dissipates kT*log2 joules of heat energy where k is Boltzmann's constant and T the absolute temperature at which the computation is performed [1]. Further in 1973, Bennett showed that zero power dissipation is possible in the logic circuits only if it is composed of reversible logic

gates since the amount of energy dissipated in a system will hold a direct relationship to the number of information bits erased during computation[2]. The copy of state of the output must be present at all times which can be obtained by using the reversible logic. The voltage-coded signals have energy of $Es= 1/2CV^2$, and this energy get dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process [22]. Reversible computation in a system can be performed only when the system comprises of reversible gates. The field of quantum computing also uses reversible logic. All quantum gates are reversible [12]. Reversible circuits can generate unique output vector (Ov) from each input vector (Iv), and vice versa, that is there is a one-to-one mapping between the input and output vectors. Thus, an nXn reversible gate can be represented as:

$$Iv= (I1,I2,I3,…….In)$$

$$Ov= (O1,O2,O3,……On)$$

Classical logic gates are irreversible since input vectors states cannot be uniquely reconstructed from output vector states. There is a number of existing reversible gates such as Fredkin gate [3,4,5], Toffoli gate (TG) [3,4] and New gate (NG) [6].

1.2 Purpose of Reversible Logic

Reversible logic are of high interest in low power CMOS design [10], optical computing [11], quantum computing [12] and nanotechnology [13]. The most remarkable application of reversible logic lies in quantum computers. A balanced reversible function has half of minterms with value 1 and another half with value 0. In a n output reversible gates, the output vectors are permutation of numbers 0 to 2n-1.

1.3 Major Concern In Reversible Logic

The input that is added to an nxk function to make it reversible is called Constant input(CI) and the outputs of the reversible circuits that are not used are called as Garbage outputs(GO). These garbage outputs are just used to preserve the circuit's reversibility. Quantum cost(QC) refers to the cost of the circuit in terms of the cost of a primitive gate. These parameters i.e. CI,GO,QC, have to be reduced while designing a reversible circuits. Some of the major problems with the reversible logic synthesis are the fanouts cannot be used and also feedback from gate output to input is not permitted. However fanout in reversible circuits is achieved using additional gates. A reversible circuit design should have minimum number of reversible logic gates.

II. PROPOSED CONCEPT IN REVERSIBLE LOGIC

This paper focus on the application of new reversible 4*4 TSG gate [23,24]. It can work singly as the reversible full adder. A novel reversible 4:2 compressor is also designed from the proposed TSG gate. In addition, the optimized

adder and 4:2 compressors are used to design the novel 16*16 reversible Wallace tree multiplier. It is observed that TSG gate achieves minimized garbage outputs and minimized reversible gates, leading to high speed and low power reversible circuits. The reversible circuits proposed and designed in this work form the basis for an ALU of a primitive quantum CPU.

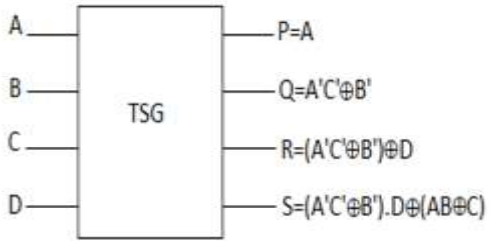

Figure 1. Proposed TSG gate

2.1 Proposed 4*4 Reversible Gate

The journalists proposed a 4*4 one through reversible gate called TS gate (TSG) which is shown in the Figure 1. It can be noted that input pattern corresponding to a particular output pattern can be uniquely determined. The proposed TSG gate is capable of implementing all Boolean functions and can also work as a reversible full adder. Figure 2 shows the implementation of the proposed gate as a reversible Full adder

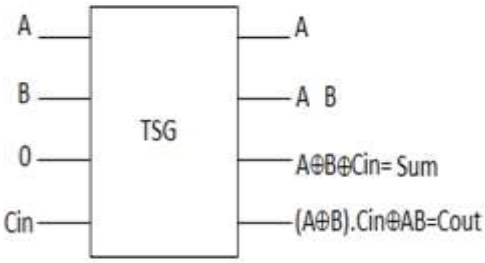

Figure 2. Proposed TSG gate as a full adder

A number of reversible full adders were proposed in [6,7,8,9]. The reversible full adder circuit in [6] requires three reversible gates(two 3*3 new gates and one 2*2 Feynman gate) and produces three garbage outputs. The reversible circuit in [7,8] requires three reversible gates (one 3*3 new gate, one 3*3 Toffoli gate and one 2*2 Feynman gate) and produces two garbage outputs. The adder circuit in [9] uses five reversible Fredkin gates and produces five garbage outputs. The proposed full adder circuit using TSG in Figure 2 uses one reversible gate that is TSG gate which produces two garbage outputs which shows that the TSG gate circuit is better than the full adder designs of [6,7,8,9] . Various full adder circuits are compared and it is given in Table 1

Table I . A Comparison of Various Reversible Full-Adder Circuits

	Number of Gates	Number of Garbage Outputs	Unit Delay
Proposed Circuit	1	2	1
Existing Circuit[6]	3	3	3
Existing Circuit[7,8]	3	2	3
Existing Circuit[9]	5	5	5

.

III. REVERSIBLE 4:2 COMPRESSOR

Weinberger in 1981 introduced 4:2 compressor and he called it as "4-2 carry save module"[16]. The 4:2 compressor structure actually compresses the five partial product bits into three in which four of the inputs are coming from the same bit position of the weight j while one bit is fed from the neighboring position j-1 (known as carry-in), The output of the 4:2 compressor consists of one bit in the position j and two bits in the position j+1. The structure of 4:2 compressor is shown in the figure 3

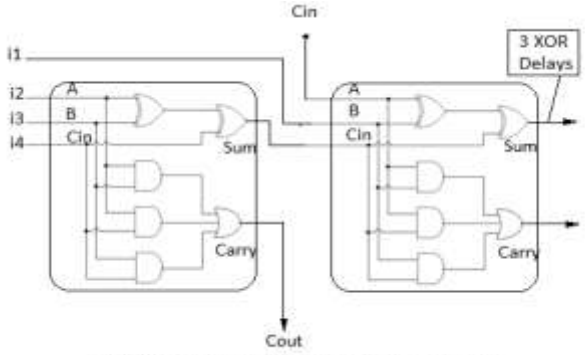

Figure 3. Logic Diagram of 4:2 Compressor

The efficiency of such a structure is higher since it reduces number of partial product bits by one half at each stage. The delay of 4:2 compressor is 3 XOR gates in series making it more efficient than using 3:2 counters i.e. full adder in a regular Wallace tree and has important feature that the interconnections between 4:2 cells follow more regular pattern than in the case of the "Wallace tree" [17,18,25]. In this paper, the 4:2 compressor is also proposed as shown in figure 4. Here, the reversible 4:2 compressor is designed from two TSG gates. The block diagram of 4:2

compressor is shown in Figure 5. Table II shows the comparison results of the 4:2 compressor using TSG with its implementation using existing reversible full adders.

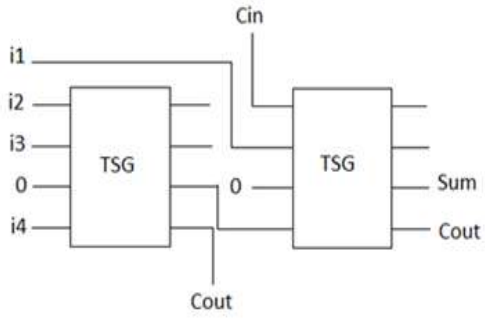

Figure 4. Proposed Reversible 4:2 Compressor designed using TSG Gate

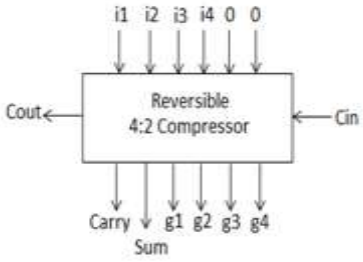

Figure 5. Block Diagram of Reversible 4:2 Compressor

Table II. A Comparison of 4:2 Compressors using Various Full adder Circuits

	Number of Reversible Gates	Number of Garbage Outputs	Unit Clock Cycle
Full Adder Using TSG	2	4	2
Existing Circuit[6]	6	6	6
Existing Circuit[7,8]	6	4	4
Existing Circuit[9]	10	10	10

IV. REVERSIBLE WALLACE TREE

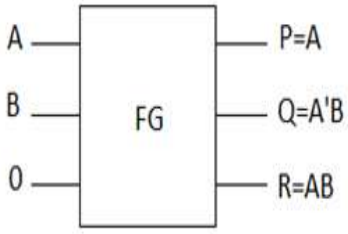

Figure 7. Use of Fredkin gates to Generate Partial Products in Parallel

A multiplication operation consists of three stages: partial products generation stage, partial product addition stage, and the final addition stage [19,20,21].The second stage is the most important and determines overall speed of the multiplier. In high speed designs, the Wallace tree construction method is usually preferred to add the partial

products in a tree-like fashion. The Wallace tree is fast since the critical path delay is proportional to the logarithm of the number of bits in the multiplier.

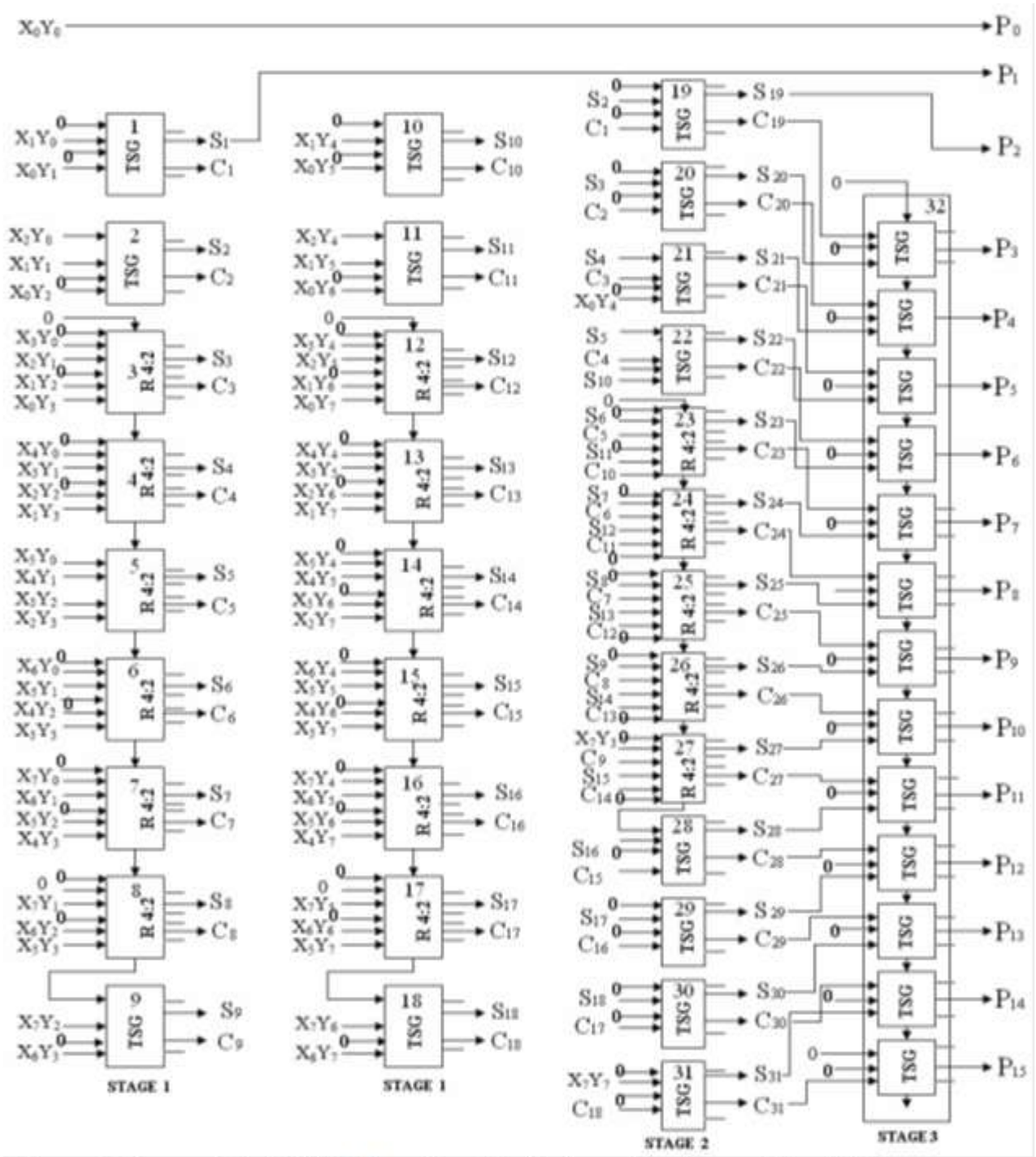

Figure 6. Reversible 8x8 Wallace Tree Multiplier using Reversible 4:2 Compressor

4.1 Reversible Wallace Tree Construction

The Figure 6 shows the circuit diagram of reversible 8x8 Wallace tree multiplier using reversible 4:2 compressor. This paper proposes reversible 16x16 Wallace tree multiplier using the reversible TSG gate, for the multiplication of two 16 bit numbers whose answer will be in 32 bit form. The method to construct the Wallace tree considers all the bits in each four rows at a time and compress them in an appropriate manner. The Wallace tree uses 4:2 compressor and full adders to compress the partial products tree. The proposed architecture can be generalized for nxn bits. The reversible full adder and 4:2 compressor designed from the reversible TSG gate are used as the basic building blocks for the design of 16x16 Wallace tree multiplier.

The generation of all partial products of the multiplication can be done in parallel by using Fredkin gates (for ANDing the bits of the multiplier and multiplicand) as shown in Figure 7.In Stage 1, as shown in Figure 6, the partial products are added using 4:2 compressors, full adders and half adders, the S and C generated of all the blocks are arranged according to their weights. In the Stage 2, the reduced partial products are again added using 4:2 compressors, full adders and half adders. The result obtained in the stage 2 is added using a parallel adder designed from TSG gates in Stage 3 to generate the product bits P0,P1,…..P31,P32.

4.2 Evaluation of the proposed Wallace Tree Multiplier

The proposed reversible 16x16 Wallace Tree Multiplier is designed from the reversible TSG gate. This is the first attempt in literature to design the reversible 16x16 Wallace Tree Multiplier. The novelties lies in the introduction of reversible TSG gate and its implementation for designing the adder and compressor, which are latter used to design reversible Wallace Tree Multiplier. There seems to be no existing counterpart in the literature and hence no comparative study is done. It has been already proved in the earlier sections that the adder and the compressor designed from the TSG gate are the most optimized one, thus making the overall architecture of the Wallace Tree Multiplier as the most optimal one.

V. CONCLUSION

The focus of this paper is the application of a new reversible 4*4 TSG gate to design the components of a primitive quantum/ reversible ALU. The TSG gate is used to design the 4:2 compressor and a optimized adder which are later used to build a novel reversible 16x16 Wallace Tree Multiplier. It is proved that the adder and 4:2 compressor and multiplier architecture designed with the TSG gate are efficient than the their counterparts, in terms of number of reversible gates and garbage outputs, resulting in the low power consuming as well as the high speed reversible circuits. All the proposed architectures are analyzed in terms of technology independent implementations. The proposed circuit can be used for building large reversible systems. Thus, this paper provides a threshold to build more complicated reversible systems.

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DESIGN OF MICROSTRIP PATCH ANTENNA

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ABSTRACT

With the constant changing of technology, frequency reconfigurable antennas are an important innovation to the RF world. The new device limits the physical space used by eliminating the need for multiple antennas. This is especially vital in mobile devices such as cell phones that receive multiple frequency bands like cellular tower reception, Wi-Fi, and GPS. The other alternative to frequency reconfigurable antennas is a wideband antenna; however, wideband antennas receive large frequency ranges introducing noise to the system. Frequency reconfigurable antennas narrow the bandwidth to specific frequencies, typically reducing the amount of noise for the signal. Wireless technology is one of the main areas of research in the world of communication systems today and a study of communication systems is incomplete without an understanding of the operation and fabrication of antennas. This was the main reason for our selecting a project focusing on this field.

Keywords: Wideband Antenna, Wifi, Gps, Wireless Technology, Bandwidth.

I INTRODUCTION

Our paper focuses on the hardware fabrication and software simulation of antenna. In order to completely understand the above it is necessary to start off by understanding various terms associated with antennas and the various types of antennas. This is what is covered in this introductory chapter.

1.1 Antenna parameters

An antenna is an electrical conductor or system of conductors Transmitter - Radiates electromagnetic energy into space Receiver - Collects electromagnetic energy from space The IEEE definition of an antenna as given by Stutzman and Thiele is, "That part of a transmitting or receiving system that is designed to radiate or receive electromagnetic waves". The major parameters associated with an antenna are defined in the following sections.

1.1.1 Antenna Gain

Gain is a measure of the ability of the antenna to direct the input power into radiation in particular direction and is measured at the peak radiation intensity. Consider the power density radiated by an isotropic antenna with input power P_0 at a distance R which is given by $S = P_0/4\pi R^2$. An isotropic antenna radiates equally in all directions, and its radiated power density S is found by dividing the radiated power by the area of the

sphere$4\pi R^2$. An isotropic radiator is considered to be 100% efficient. The gain of an actual antenna increases the power density in the direction of the peak radiation:

Gain is achieved by directing the radiation away from other parts of the radiation sphere. In general, gain is defined as the gain-biased pattern of the antenna.

$$S(\theta,\phi) = \frac{P_0 G(\theta,\phi)}{4\pi R^2} \qquad \text{power density}$$

$$U(\theta,\phi) = \frac{P_0 G(\theta,\phi)}{4\pi} \qquad \text{radiation intensity}$$

1.1.2 Antenna Efficiency

The surface integral of the radiation intensity over the radiation sphere divided by the input power P_0 is a measure of the relative power radiated by the antenna, or the antenna efficiency.

$$\frac{P_r}{P_0} = \int_0^{2\pi}\int_0^{\pi} \frac{G(\theta,\phi)}{4\pi} \sin\theta \, d\theta \, d\phi = \eta_e \qquad \text{efficiency}$$

where *Pr* is the radiated power. Material losses in the antenna or reflected power due to poor impedance match reduce the radiated power.

1.1.3 Effective Area

Antennas capture power from passing waves and deliver some of it to the terminals. Given the power density of the incident wave and the effective area of the antenna, the power delivered to the terminals is the product.

$$P_d = SA_{\text{eff}}$$

For an aperture antenna such as a horn, parabolic reflector, or flat-plate array, effective area is physical area multiplied by aperture efficiency. In general, losses due to material, distribution, and mismatch reduce the ratio of the effective area to the physical area. Typical estimated aperture efficiency for a parabolic reflector is 55%. Even antennas with infinitesimal physical areas, such as dipoles, have effective areas because they remove power from passing waves.

1.1.4 Return Loss

It is a parameter which indicates the amount of power that is "lost" to the load and does not return as a reflection. Hence the RL is a parameter to indicate how well the matching between the transmitter and antenna has taken place. Simply put it is the S11 of an antenna. A graph of s11 of an antenna vs frequency is called its return loss curve. For optimum working such a graph must show a dip at the operating frequency and have a minimum dB value at this frequency.

1.1.5 Input Impedance

The input impedance of an antenna is defined as "the impedance presented by an antenna at its terminals or the ratio of the voltage to the current at the pair of terminals or the ratio of the appropriate components of the electric to magnetic fields at a point". Hence the impedance of the antenna can be written as given below.

$$Z_{in} = R_{in} + jX_{in}$$

where Z_{in} is the antenna impedance at the terminals

R_{in} is the antenna resistance at the terminals

X_{in} is the antenna reactance at the terminals

The imaginary part, X_{in} of the input impedance represents the power stored in the near field of the antenna. The resistive part, R_{in} of the input impedance consists of two components, the radiation resistance R_r and the loss resistance R_L. The power associated with the radiation resistance is the power actually radiated by the antenna, while the power dissipated in the loss resistance is lost as heat in the antenna itself due to dielectric or conducting losses.

1.1.6 Antenna Factor

The engineering community uses an antenna connected to a receiver such as a spectrum analyzer, a network analyzer, or an RF voltmeter to measure field strength E. Most of the time these devices have a load resistor ZL tha matches the antenna impedance.

We relate this to the antenna effective height:

$$\mathrm{AF} = \frac{E_i}{V_{\mathrm{rec}}} = \frac{2}{h}$$

AF has units meter^{-1} but is often given as dB(m^{-1}). Sometimes, antenna factor is referred to the open-circuit voltage. We assume that the antenna is aligned with the electric field; in other words, the antenna polarization is the electric field component measured.

$$AF = \sqrt{\frac{\eta}{Z_L A_{\text{eff}}}} = \frac{1}{\lambda}\sqrt{\frac{4\pi}{Z_L G}}$$

This measurement may be corrupted by a poor impedance match to the receiver and any cable loss between the antenna and receiver that reduces the voltage and reduces the calculated field strength.

II MICROSTRIP PATCH ANTENNA SCTRUCTURE

A microstrip patch antenna (MPA) consists of a conducting patch of any planar or non-planar geometry on one side of a dielectric substrate with a ground plane on other side. It is a popular printed resonant antenna for narrow-band microwave wireless links that require semi hemispherical coverage. Due to its planar configuration and ease of integration with microstrip technology, the microstrip patch antenna has been heavily studied and is often used as elements for an array. A large number of microstrip patch antennas have been studied to date. An exhaustive list of the geometries along with their salient features is available. The rectangular and circular patches are the basic and most commonly used microstrip antennas. These patches are used for the simplest and the most demanding applications. Rectangular geometries are separable in nature and their analysis is also simple. The circular patch antenna has the advantage of their radiation pattern being symmetric. A rectangular microstrip patch antenna in its simplest form is shown in Figure 1.1

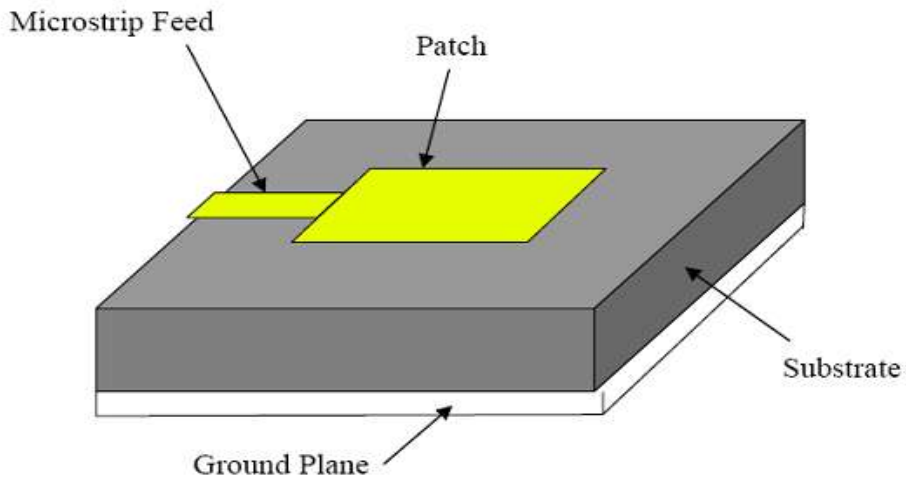


Figure 2.1 Structure of Microstrip patch antenna

The Microstrip antennas are the present day antenna designer's choice. Low dielectric constant substrates are generally preferred for maximum radiation. The conducting patch can take any shape but rectangular and

circular configurations are the most commonly used configuration. Other configurations are complex to analyze and require heavy numerical computations. A Microstrip antenna is characterized by its Length, Width, Input impedance, and Gain and radiation patterns.

2.1 Characteristics of Microstrip Patch Antenna

i) VSWR

VSWR stands for Voltage Standing Wave Ratio, and is also referred to as Standing Wave Ratio (SWR). VSWR is a function of the reflection coefficient, which describes the power reflected from the antenna. The VSWR is always a real and positive number for antennas. The smaller the VSWR is, the better the antenna matched to the transmission line and the more power is delivered to the antenna. The minimum VSWR is 1.0. In this case, no power is reflected from the antenna, which is ideal.

ii) Radiation Pattern

The patch's radiation at the fringing fields results in a certain far field radiation pattern. This radiation pattern shows that the antenna radiates more power in a certain direction than another direction. The antenna is said to have certain directivity. This is commonly expressed in dB. An estimation of the expected directivity of a patch can be derived with ease. The fringing fields at the radiating edges can be viewed as two radiating slots placed above a ground plane. Assuming all radiation occurs in one half of the hemisphere, this results in 3 dB directivity. This case is often described as a perfect front to back ratio.

iii) Gain

Gain is a measure of the ability of the antenna to direct the input power into radiation in particular direction and is measured at the peak radiation intensity.An isotropic radiator is considered to be 100% efficient. The gain of an actual antenna increases the power density in the direction of the peak radiation.

iv) Input Impedence

The input impedance of an antenna is defined as “the impedance presented by an antenna at its terminals or the ratio of the voltage to the current at the pair of terminals or the ratio of the appropriate components of the electric to magnetic fields at a point”. Hence the impedance of the antenna can be written as given below.

$$Z_{in} = R_{in} + jX_{in}$$

where Z_{in} is the antenna impedance at the terminals

R_{in} is the antenna resistance at the terminals

X_{in} is the antenna reactance at the terminals

2.2 Shapes of Patch

In order to simplify analysis and performance prediction, the patch is generally square, rectangular, circular, triangular, elliptical or some other common shape as shown in Figure 2. For a rectangular patch, the length L of the patch is usually $0.3333\lambda_o < L < 0.5\lambda_o$, where λ_o is the free-space wavelength. The patch is selected to be very thin such that $t << \lambda_o$ (where t is the patch thickness). The height h of the dielectric substrate is usually $0.003\ \lambda_o \leq h \leq 0.05\ \lambda_o$. The dielectric constant of the substrate (ε_r) is typically in the range $2.2 \leq \varepsilon_r \leq 12$.

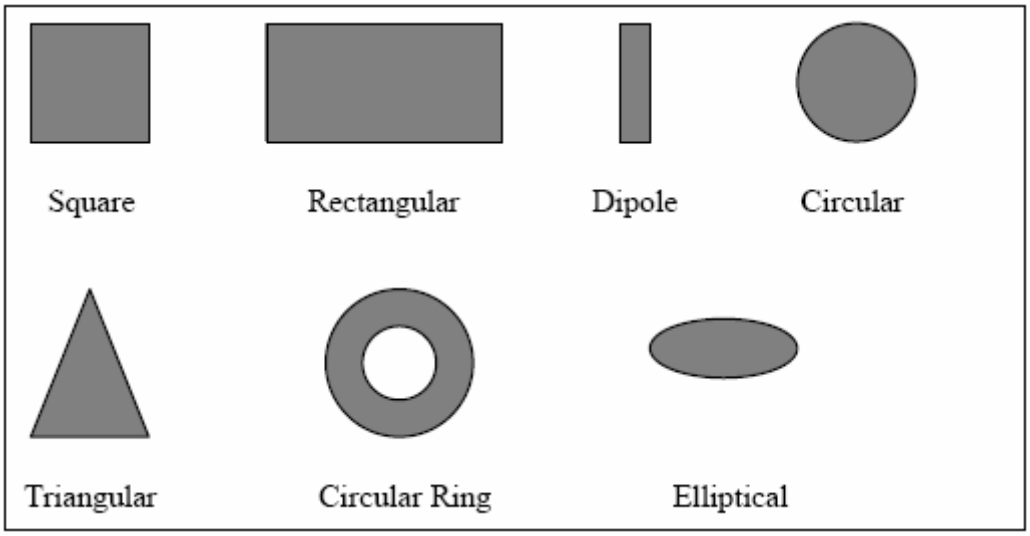


Figure -2.2 – Typical patch shapes

A patch radiates from fringing fields around its edges. The situation is shown in figure 3.3. Impedance match occurs when a patch resonates as a resonant cavity. When matched, the antenna achieves peak efficiency. A normal transmission line radiates little power because the fringing fields are matched by nearby counteracting fields. Power radiates from open circuits and from discontinuities such as corners, but the amount depends on the radiation conductance load to the line relative to the patches. Without proper matching, little power radiates. The edges of a patch appear as slots whose excitations depend on the internal fields of the cavity. A general analysis of an arbitrarily shaped patch considers the patch to be a resonant cavity with metal (electric) walls of the patch and the ground plane and magnetic or impedance walls around the edges.

For good antenna performance, a thick dielectric substrate having a low dielectric constant is desirable since this provides better efficiency, larger bandwidth and better radiation. However, such a configuration leads to a larger antenna size. In order to design a compact Microstrip patch antenna, higher dielectric constants must be used which are less efficient and result in narrower bandwidth. Hence a compromise must be reached between antenna dimensions and antenna performance.

2.3 Feed Techniques

Microstrip patch antennas can be fed by a variety of methods. These methods can be classified into two categories- contacting and non-contacting. In the contacting method, the RF power is fed directly to the

radiating patch using a connecting element such as a microstrip line. In the non-contacting scheme, electromagnetic field coupling is done to transfer power between the microstrip line and the radiating patch. The four most popular feed techniques used are the microstrip line, coaxial probe (both contacting schemes), aperture coupling and proximity coupling (both non-contacting schemes)

. 2.4.1 Microstrip Coaxial Feed

In this type of feed technique, a conducting strip is connected directly to the edge of the microstrip patch as shown in Figure 3.2. The conducting strip is smaller in width as compared to the patch and this kind of feed arrangement has the advantage that the feed can be etched on the same substrate to provide a planar structure.

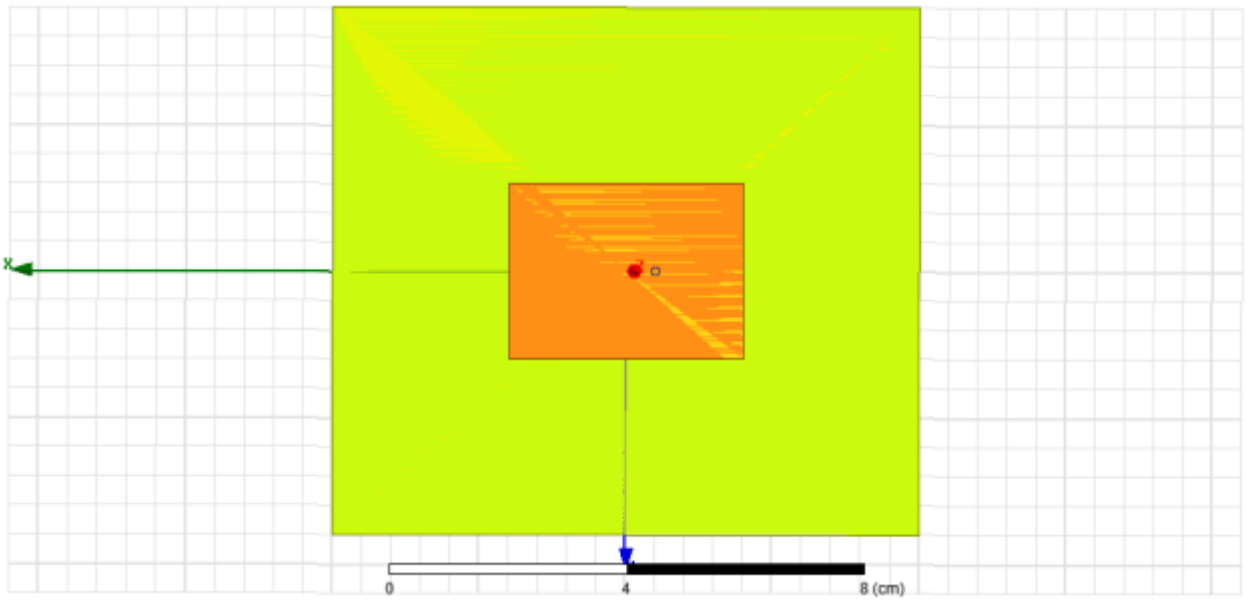


Figure:2.3 Microstrip patch: Top view

The purpose of the inset cut in the patch is to match the impedance of the feed line to the patch without the need for any additional matching element. This is achieved by properly controlling the inset position. Hence this is an easy feeding scheme, since it provides ease of fabrication and simplicity in modeling as well as impedance matching. However as the thickness of the dielectric substrate being used, increases, surface waves and spurious feed radiation also increases, which hampers the bandwidth of the antenna. The feed radiation also leads to undesired cross polarized radiation.

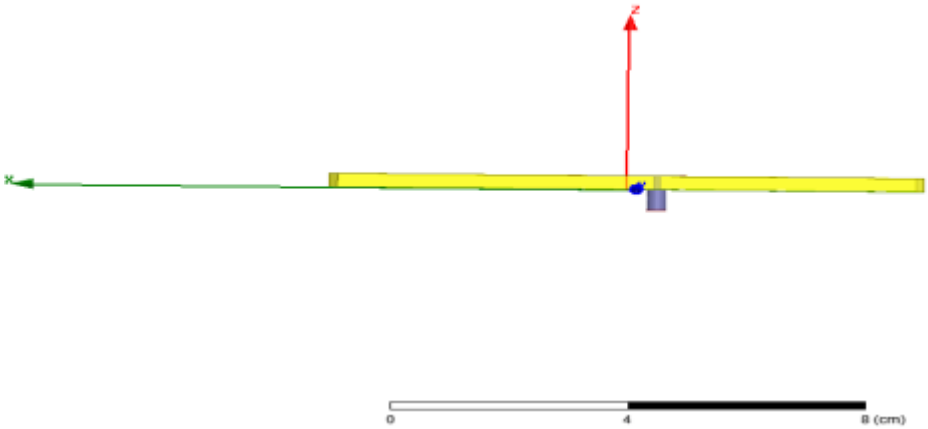


Figure:3.4 Microstrip patch: Lateral view

2.5 Applications of Microstrip Patch Antennas

Microstrip patch antennas are increasing in popularity for use in wireless applications due to their low-profile structure. Therefore they are extremely compatible for embedded antennas in handheld wireless devices such as cellular phones, pagers etc. The telemetry and communication antennas on missiles need to be thin and conformal and are often microstrip patch antennas. Another area where they have been used successfully is in satellite communication.

2.6 Advantages and Disadvantages of Patch Antennas

Some of their principal advantages of microstrip patch antennas are given below:

• Light weight and low volume.
• Low profile planar configuration which can be easily made conformal to host surface.
• Low fabrication cost, hence can be manufactured in large quantities.
• Supports both, linear as well as circular polarization.
• Can be easily integrated with microwave integrated circuits (MICs).
• Capable of dual and triple frequency operations.
• Mechanically robust when mounted on rigid surfaces.

Microstrip patch antennas suffer from a number of disadvantages as compared to conventional antennas. Some of their major disadvantages are given below:

• Narrow bandwidth
• Low efficiency
• Low Gain
• Extraneous radiation from feeds and junctions
• Poor end fire radiator except tapered slot antennas
• Low power handling capacity.
• Surface wave excitation

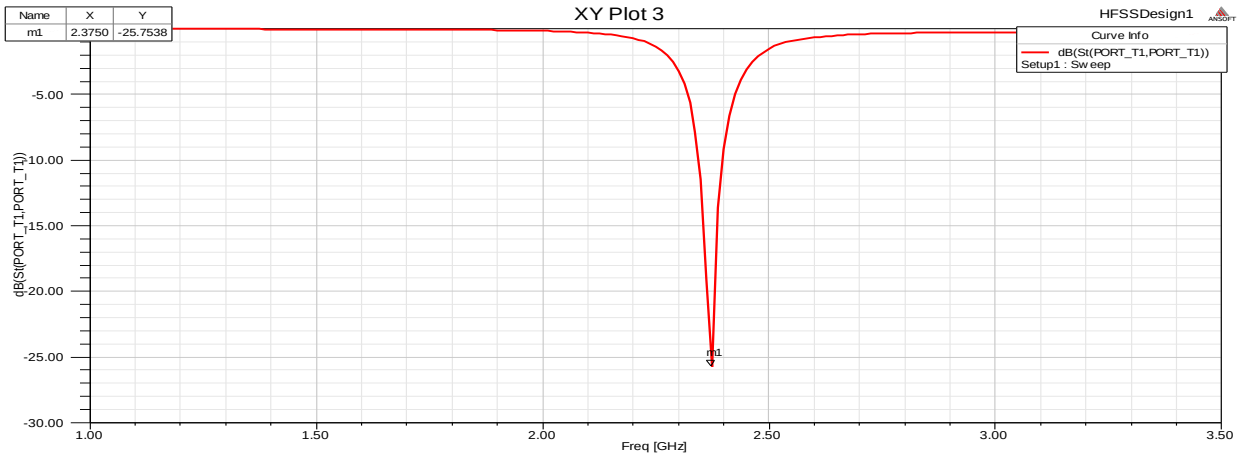
Microstrip patch antennas have a very high antenna quality factor (Q). Q represents the losses associated with the antenna and a large Q leads to narrow bandwidth and low efficiency. Q can be reduced by increasing the

thickness of the dielectric substrate. But as the thickness increases, an increasing fraction of the total power delivered by the source goes into a surface wave. This surface wave contribution can be counted as an unwanted power loss since it is ultimately scattered at the dielectric bends and causes degradation of the antenna characteristics. However, surface waves can be minimized by use of photonic bandgap structure. Other problems such as low gain and low power handling capacity.

III SIMULATION OF MICROSTRIP PATCH ANTENNA

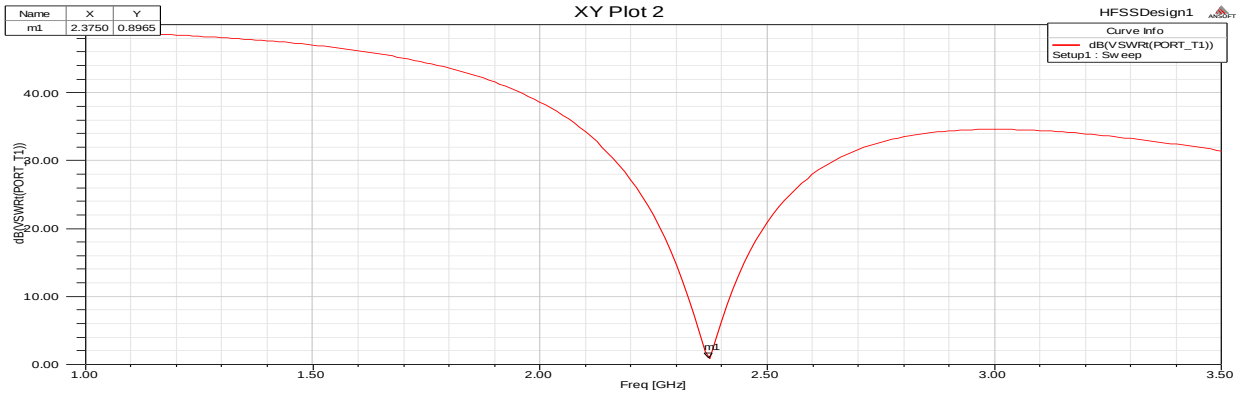
3.1 Simulation

3.1.1 Return Loss Graph I



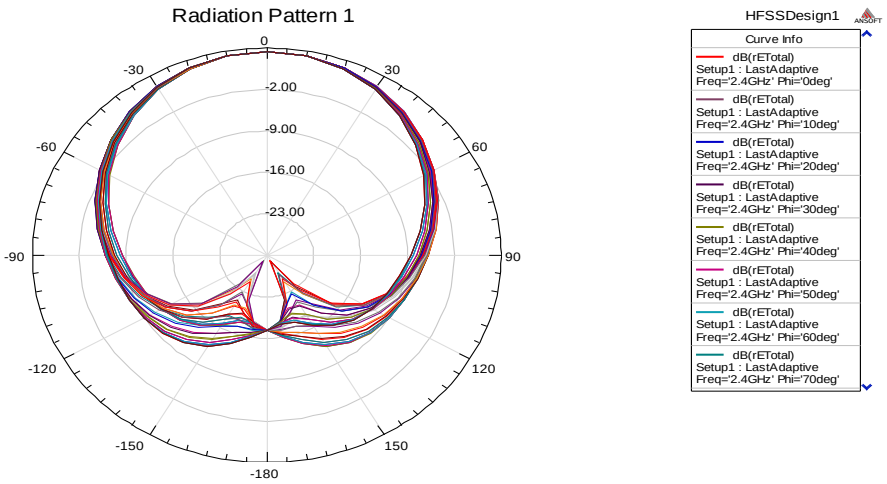
3.1 Figure:Return loss graph I

3.1.2 Return Loss Graph II



3.2 Figure:Return loss graph II

3.1.3 Radiation Pattern



3.3 Figure:Radiation Pattern

3.1.4 3-D POLAR PLOT

3.4 Figure: 3-D POLAR PLOT

IV CONCLUSION AND RESULT

Testing with MEMS switches will follow, but at the moment the antenna system behaves almost as intended beyond the resonant frequency locations. However, a larger bandwidth could have fixed these problems. This could be done with a thicker substrate or lower dielectric constant.Determining the cause of the change in resonant frequency will come with later testing.

4.1 Recommendations

The design behind the reconfigurable patch antenna has many possibilities for future work. First off, circular polarization can be added by truncated corners, slots, etc. It was dropped from the project due to time constraints and complexity it presented. Some preliminary work was done to show it was feasible, but the goal was to produce a working frequency reconfigurable antenna by the end of the semester. In addition, a single stub or double stub impedance matching network could be used instead of inset feed matching. While not entirely necessary, at different application frequencies these impedance matching networks will give more accurate matching for each resonant frequency. The downfall of these matching networks compared to inset feed matching is the complexity and physical size added into the project. For final fabrication and design of the patch antenna, due to variances between simulations and tests, it is suggested that multiple designs are made of the antenna. For these designs some patches should be made to resonant slightly higher than desired, some at desired, and some below desired during simulations. These, when fabricated, will help determine the final dimensions to be used for final product fabrication and thus will help eliminate any variances, like the ~60Mhz differences we noticed.

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AUTOMATIC POWER FACTOR IMPROVEMENT USING EMBEDDED SYSTEM

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ABSTRACT

The objective of this project is to moniter and control the cosine angle between the voltage and current in order to save the electric energy.This project is very useful in the industries where heavy inductive loads are used.If the powerfactor is less than unity the line current is greater and increases the KVA demand.This attracts penalty imposed by Electricity Board.

Keywords: Electric Energy, Power Factor, Cosine Angle, KVA.

I.INTRODUCTION

1.1 Need of Project

This project is used to monitor and control the cosine angle between the voltage and current in order to save the electric energy. If the power factor is less than unity, the line current is greater than the load current, which causes heating of switch contacts, cables etc. As also it causes to rise in reactive power, the KVA demand increases.

This leads to double payment to EB office and this leads to penalty charges. So this project is very useful to the industries where inductive loads are used.

At present maximum number of industries use power factor controller to maintain the power factor. Those power factor controller use normal relays in their circuits for the switching purposes. Since those normal relays have a low switching speed, the power factor cannot be controlled continuously without steps.

When compared to our circuit design the normal relay circuit cost is greater. The relay will have some chattering in its contacts and they will get damaged soon. In industries the power factor control circuit uses relays for switching. By understanding the problem of the relay circuit we made a different design. In this project we have replaced the relay by a Thyrister.

II. OVER VIEW OF AUTOMATIC POWER FACTOR IMPROVEMENT USING EMBEDDED SYSTEM

2.1 Block Diagram

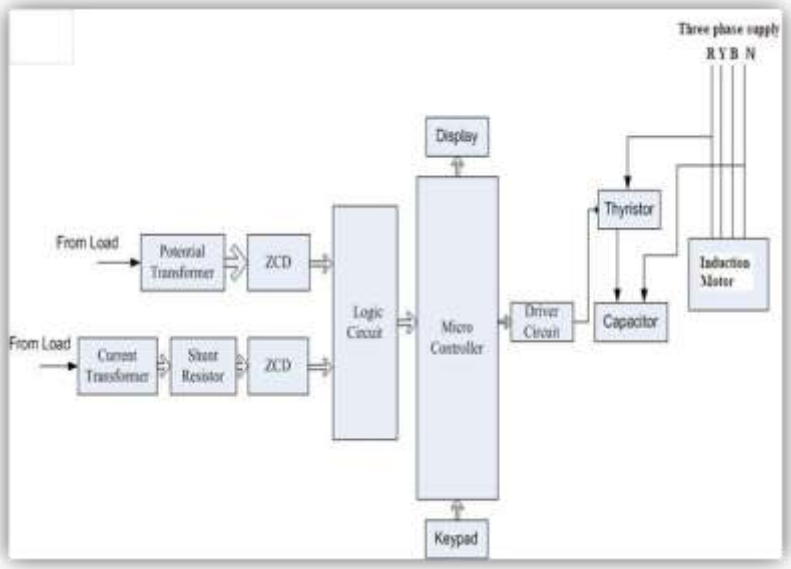

Fig 1.1 Block diagram of Automatic Power Factor Improvement Using Embedded System

2.2 Block Diagram Description

1.Potential transformer

Voltage to the motor is measured with the help of a potential transformer. The potential transformer will convert the mains supply voltage to low voltage ac. That ac voltage is given to zero crossing detectors

2. Current transformer

The current transformer will convert the load current in to lower values that current output will be converted in to voltage with the help of the shunt resistor. Then the corresponding the ac voltage is given to zcd.

3. Zero crossing detectors

The zero crossing detectors are used to convert the input sine wave signal to corresponding square wave signal. For power factor measurement, the sensing of ct and pt are taken from any one of the phases and given to zero cross detector (zcd) and both voltage and current are converted square wave, ic741 compare the square wave and the resultant output is given to the micro controller.

4. Logic circuit

In this logic circuit an ex-or gate is used. This ex-or gate is used for calculation. This intakes the output from the two comparators and makes a calculation. Then the square wave signal is given to logic circuit in order to find timing between the two pulses. Then the corresponding pulse output is given to microcontroller.

5. Micro controller

The microcontroller is the flash type reprogrammable microcontroller in which we have already programmed with our objectives the microcontroller received the corresponding square pulse from the logic circuit and performs the mathematical calculation on the pulse to find the cosine angle.

6. Lcd display

2x16 lcd display used to display the power factor value.

7. Driver circuit

This circuit is used to drive the thyristor.

8. Thyristor

Thyristor is a semiconductor switching device and it is used for adding and cutting the capacitor.

9. Capacitor

The capacitor is mainly used to improve the power factor when normal power factor is going lagging condition.

III.WORKING PRINCIPLE

Voltage to the motor is measured with the help of a potential transformer. The potential transformer will convert the mains supply voltage to low voltage AC. That AC voltage is given to zerocrossing detectors. Current consumed by the motor is measured with the help of a current transformer.

The current transformer will convert the load current in to lower values that current output will be converted in to voltage with the help of the shunt resistor. Then the corresponding the AC voltage is given to Zero crossing detectors.

The zero crossing detectors are used to convert the input sine wave signal to corresponding square wave signal. Then the square wave signal is given to logic circuit in order to find timing between the two pulses. Then the corresponding pulse output is given to microcontroller.

Here the microcontroller is already programmed with our objectives. The microcontroller receives the corresponding square pulse from the logic circuit and performs the mathematical calculation on the pulse to find the cosine angle.

The cosine value is displayed on the LCD display which is equal to the monitored power factor.If the monitored power factor is less then unity, then the microcontroller activates the Thyrister driver circuit.

The fixed capacitor is connected across the Thyrister output terminal. When Thyrister output terminal is shorted through the capacitor the lagging angle is compensated through lading angle due to the capacitor. If the cosine angle crosses the unity and moves towards the leading angle suddenly the capacitor is cut off and the angle moves towards the unity. Thus the power factor is maintained efficiently

IV.TEST RESULTS

4.1 Load Test (Without Capacitor)

Load status	Line voltage	Line current	Input power	cosφ	% ofŋ
No load	230	0.5	20	0.2	-
Full load	230	0.75	130	0.7	85

Table:1.1 Test results

4.2 Load Test (With Capacitor)

Load status	Line voltage	Line current	Input power	cosφ	% ofŋ
No load	230	0.5	20	0.9	-
Full load	230	0.75	130	0.9	89

Table:1.2 Test results

4.3 Bar Chart

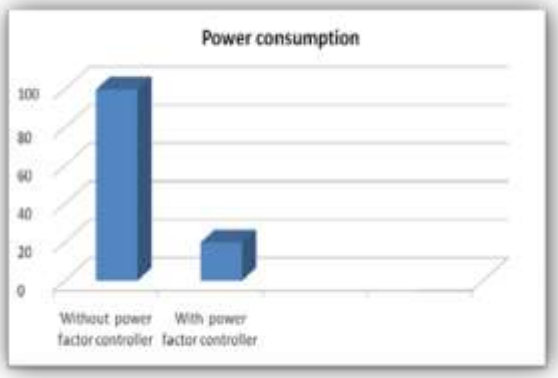

Fig:1.2 Bar chart

From the bar chart we can understand that when an industry run without a power factor controller the power consumption will be high and so much loss will occur to the EB and to the industry. By introducing the power factor controller the power will be 80% saved and power losses will be no more.

4.4 Graph

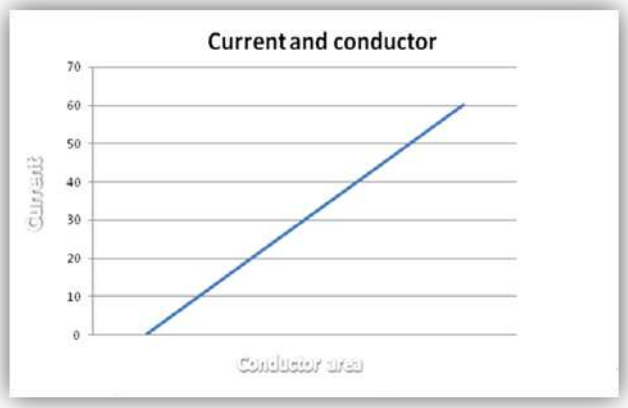

Fig:1.3 Graph

The above graph shows relation between the current and the conductor. From the graph we can know that when the current increases the conductor size also increases.

Thus when a power factor controller is fixed the current in the line is too minimum so the size of conductors will reduces and the initial cost also reduced.

V. DRAWBACK

5.1 HARMONIC DISTORTION

1. The Harmonic Problem

Any device with non-linear operating characteristics can produce harmonics in your power system. If you are currently using equipment that can cause harmonics or have experienced harmonic related problems, capacitor reactor or filter bank equipment may be the solution. Harmonic distortion and related problems in electrical power systems are becoming more and more prevalent in electrical distribution systems.

2.Problems Created by Harmonics

- Excessive heating and failure of capacitors, blowing of capacitor fuses, heating of transformers, motors and fluorescent lighting ballasts, etc.
- Nuisance tripping of circuit breaker or blown fuses
- Presence of the third harmonic & multiples of the 3rd harmonic in neutral grounding systems may require the de-rating of neutral conductors
- Noise from harmonics that lead to erroneous operation of control system components
- Damage to sensitive electronic equipment
- Electronic communications interference

The following is a discussion of harmonics; the characteristics of the problem; and a discussion of our solution.

3.Harmonic Solution

Capacitor, De-tuned Capacitor & Filter Bank products from ABB Control:

Asea Brown Boveri (ABB) is the world's largest manufacturer of dry type low voltage capacitors. ABB Control utilizes this experience in recommending three options to solve the problems associated with applying capacitors to systems having harmonic distortion:

1. Apply the correct amount of capacitance (kvar) to the network to avoid resonance with the source. This may be difficult, especially in automatic systems as the capacitance is always changing.
   This solution usually means connecting less capacitance to the system than is actually needed for optimum power factor correction.
2. Install reactors in series with capacitors to lower the resonance below critical order harmonics; i.e., 5th, 7th, 11th & 13th. This design tunes the resonant frequency of the system well below the 5th harmonic and is called a detuned filter bank.
   This solution allows the capacitors to operate in a harmonic environment.
3. Filters are recommended if a problem exists with harmonic distortion before the application of power factor correction, or if the harmonic distortion is above the limits recommended in IEEE 519, Guide for Harmonic Control and Reactive Compensation of Static Power Converters.
   Tuned filters sized to reduce the harmonic distortion at critical frequencies have the benefits of correcting the power factor and improving the network power quality.

VI.ADVANTAGES

- Low power consumption.

- The parameters are acquired effectively.
- High Efficiency.
- Long life of machines.
- Money will be saved.
- Maintenance is less.
- Much useful for industries.

VI.CONCLUSION

Now days, in industries 70% of motors are induction motors. In this motor the no load power factor will be low due to the magnetizing current. And so in industries large amount of loss occurs.This project will be helpful in maintaining the power factor of an industry. By adopting this project, mutual benefit is gained over consumer and Electricity Board. We have given clear details about each and every section of this project. The project is economically beneficial one.

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EXPERIMENTAL AND COMPUTATIONAL SIMULATION OF PRODUCING ULTRA-FINE GRAIN STRUCTURE PROCESSED BY CGP

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ABSTRACT

In this research the constrained groove pressing (CGP) process as a severe plastic deformation (SPD) method was applied on commercially pure aluminum plates. According to the principle of CGP, a material is subjected to repetitive shear deformation by utilizing asymmetrically grooved dies and flat dies which are constrained by a channel. Each complete groove pressing pass consists of four pressing operation steps. Considering the geometry of the die, in each complete pass, a large amount of strain is induced into the specimen. In the present research the effects of the deformation passes on the mechanical properties of the specimens were tested by micro hardness tests. In addition, in order to investigate the material flow along the grooves in the CGP process, the finite element simulations were carried for one of the process. Our approach involves computational simulation of the entire synthesis process for the optimization. Results show that the flow stress of the material and its hardness are affected by the number of passes. Post process of the finite element analysis showed that the real state of the CGP process is a combination of plane stress and plane strain conditions.

Keywords: Aluminum, CGP, Finite Element Analysis, Mechanical Properties, UFG

I. INTRODUCTION

Structural changes in materials subjected to SPD and their effect on properties have been investigated for more than two decades. In the last ten years, our knowledge of the governing phenomena has been largely extended. However, the SPD-processed metals have ultra-fine grained structures that cannot be obtained through conventional thermo-mechanical processes. As a result, the SPD metals exhibit unique and excellent properties such as high strength, compared with the conventional materials having a coarse grain size of over several tens of micrometers. Since SPD was demonstrated as an effective approach to produce UFG metals, extensive research has been carried out to develop SPD techniques and to establish processing parameters and routes for fabricating UFG metals and alloys with enhanced properties. ECAP [3-9, 21-22] and ARB [3-6] are the SPD techniques that were first used to produce nanostructured metals and alloys possessing sub micrometer or even nano-sized grains. There were many researches were carried out to trim down the drawbacks of the earlier ECAP and ARB processes by changing routes and die angles. Theses ECAP and ARB techniques directs the evolution of other SPD technique like HPT [10]. This nonstop work on researching SPD techniques has a recent

development of a number of other SPD processes like HPT [12,14], TW [13], MDF [15] and RCS [16-17]. Over the past decade, new methods such as constrained groove pressing (CGP) [9] and constrained groove rolling (CGR) [10] have been investigated. These two new methods have been capable of producing plate-shaped ultrafine-grained materials. CGP as a severe plastic deformation was initially proposed by Shin et al. [9]. Based on the principle of CGP, a material is subjected to repetitive shear deformation under plastic strain deformation conditions by utilizing asymmetrically grooved dies and flat dies through alternate pressing [11,12]. In this field a number of numerical investigations have also been made. Park et al. investigated the GP process by use of FEM. In another research, Yoon et al. studied the plastic deformation and the strain localization in this process by means of 2D finite element simulation. They neglected the plastic deformation along the groove direction [13]. Present scenario, SPD techniques are emerging from the domain of laboratory-scale research into commercial production of various ultra-fine-grained materials. It is only the matter of time to unearth new and superior SPD technique.

In this present study the mechanical behavior of, the commercially pure aluminum sheets under the annealed conditions were selected to investigate the mechanical properties of the deformed material. The hardness and the flow stress were studied as a function of the number of passes. For analytical purposes, the plastic deformation behavior of the specimen during the first groove pressing step was also simulated using the Finite Element method.

II. GRAIN REFINEMENT

At room temperature, the yield stress of metallic materials increases with the decreasing grain size. This is known as the Hall-Petch relationship. One of the possible techniques, used to obtain small grains in metals, consist in applying a large level of plastic strain to a course-grain precursor. A simultaneous accumulation of localized dislocations and increase in the lattice misorientation are responsible for crystal subdivision and subsequently developed submicroscopic grains. However, some researches reveal that, particularly in pure metals, there exists a limit below which reducing the grain size further results in shifting in the deformation mechanism into a different yet unknown mechanism of plastic flow.

Strain hardening, which is defined as a change in flow stress with strain, is caused by the interaction of dislocations with each other and other defects. The traditional picture of plastic deformation behavior and its mechanical response (i.e. hardness increase due to work hardening) seem to be no longer valid while reducing grain size far into submicron scale. For example, in nanocrystalline Cu, deformation behavior falls into two patterns. Using molecular dynamic simulations, there has been found [4] that, if the crystal size is small enough (in Cu it is for the grain size from 5 nm to 50 nm), grain boundary sliding starts to dominate the deformation behavior. This result was recently confirmed in nanocrystalline Ni experimentally [14]. It was found that electrodeposited nanocrystalline Ni, subjected to plastic strain, did not build up a residual dislocation network.

Taking into account the recent literature announcements on deformation behavior, one can split polycrystalline metals into the following grain size regimes. For sizes greater than1000nm, traditional mechanisms determine deformation (coarse-grained polycrystalline metals). In the range from 1000 nm down to 30 nm, disordered grain boundaries begin to dominate the mechanical behavior (ultrafine-grained polycrystalline metals). This transition becomes much more evident below100 nm. At smaller scales, the atomic sliding at grain boundaries increases, leading to virtually no further work hardening of the plastically deformed metal. The introduced

classes of metals have been shown in Fig. 1, revealing the type of mechanical response and characteristics of dislocation activity. The supposed grain size, dg, for the change in the deformation mechanism, was indicated with a number of tick marks.

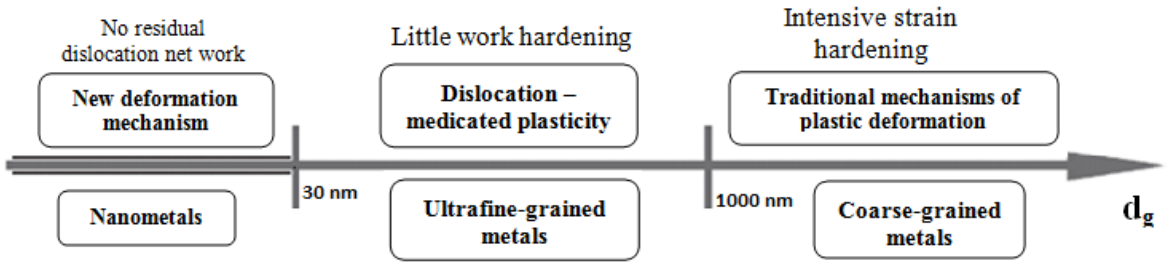


Fig.1 Classification of Polycrystalline Metals According To the Grain Size

Data shown in Fig. 1 have one important implication for grain refinement in metals via plastic strain. Plastic working remains efficient in terms of producing small grain sizes only in the range down to 30 nm for most metals and their alloys. Concluding further, one can state that, employing metal forming, it is possible to fabricate only so called ultra-fine grained (UFG) metals, not even touching desirable nanometals. However, new findings on the mechanism of plastic flow of nanometals could shed more light and open the gate for metal forming also in this range. For now, the nanometals' territory has been restricted to new synthesis-based methods of materials fabrication.

There are a lot of peculiarities affecting the grain refinement obtained by severe plastic deformation. Alloys are more responsive to intensive straining than pure metals, which results in finer grains. This effect, however, requires the application of larger strain. The rate of grain refinement can be increased by the presence of coarse second-phase particles [6,7]. UFG metals exhibit exceptionally high strength and reduced, but reasonable ductility. As stated in Fig. 1, they cannot go through strain hardening and are prone to flow localization during forming. However, by choosing appropriate parameters of the grain refinement process, it is possible to remove or delay the plastic instabilities. Usually researches aiming at grain refinement do not take into consideration the influence of strain rate. Dislocations [16] generated under static conditions of deformation run through small grains without virtually any disturbance in their movement. Dislocations move with a constant rate which depends only on the mechanical properties of metal. So performing high speed working is the only way to increase probability of collisions between dislocations and achieving a higher rate of strain hardening [9].The process parameter interactions should be studied further and the traditional picture of the metal forming technology should be revised in the light of latest findings on grain refinement. It is worth emphasizing that all metallic materials respond to severe straining in basically the same way. Technically, nanostructure can be achieved locally by a number of processes.

Grain refinement by severe plastic deformation implies the creation of new high angle grain boundaries. The creation of high angle boundaries is a result of grain subdivision mechanisms. Various SPD processes such as ECAP, ARB, HPT, HE, TW and RCS are well investigated for producing ultra grained metals. These investigations shows metals produced by these processes have very small average grain size of less than 1µm, with grain boundaries of mostly high angle mis-orientation. In the optical microstructure of metals over 5 passes of the ECAP processes shows the strong filamentary microstructure development with an increased number of

passes. In aluminum and aluminum alloys submicron grain sizes can be developed by using ECAP processes. Here the ECAP processed metals shows good agreement with the standard Hall-Petch relationship i.es, microstructure refinement and mechanical properties improvement. [3-5].

Dynamic strain aging achieved on Al 6061 alloy processed through ECAP having parallel channels resulted in the formation of nanodimensional particles. In the longitudinal section of the material, the grains are somewhat elongated along the direction of the shearing strain and in the transverse section, equiaxed grains were predominated. This causes the material leads to UFG structure containing grain boundaries with a predominantly high angle misorientations. Because of these changes considerably higher strength and better plasticity was achieved as compared to material after a standard strengthening treatment. Materials having low Stacking Fault Energy (SFE) such as Al and Cu can be easily downed to nanometer scale [7, 8].

In ARB processed materials it was noted that the evolution of microstructure and increase in mis-orientation of boundaries were much faster than those when using conventional rolling. HPT is another implementation of the SPD on metals and it can be successfully applied to refine microstructure in metals, alloys and recently in composites and semiconductors. HPT can refine the final grain size 100nm or less, but the drawback of this technique is the samples processed are invariably small in size and this effective grain refinement technique used so far in laboratory experimentation [9, 10].

III. CGP DEVELOPMENTS

Constrained groove pressing (CGP) is a processing method, in which a metal is subjected to an intense Plastic deformation through repeated dominant shearing and pressing (flattening) of plate.In2001, Zhu et al. described an SPD method based on the repetitive corrugating and straightening (RCS) which is more known now as CGP [1–3].

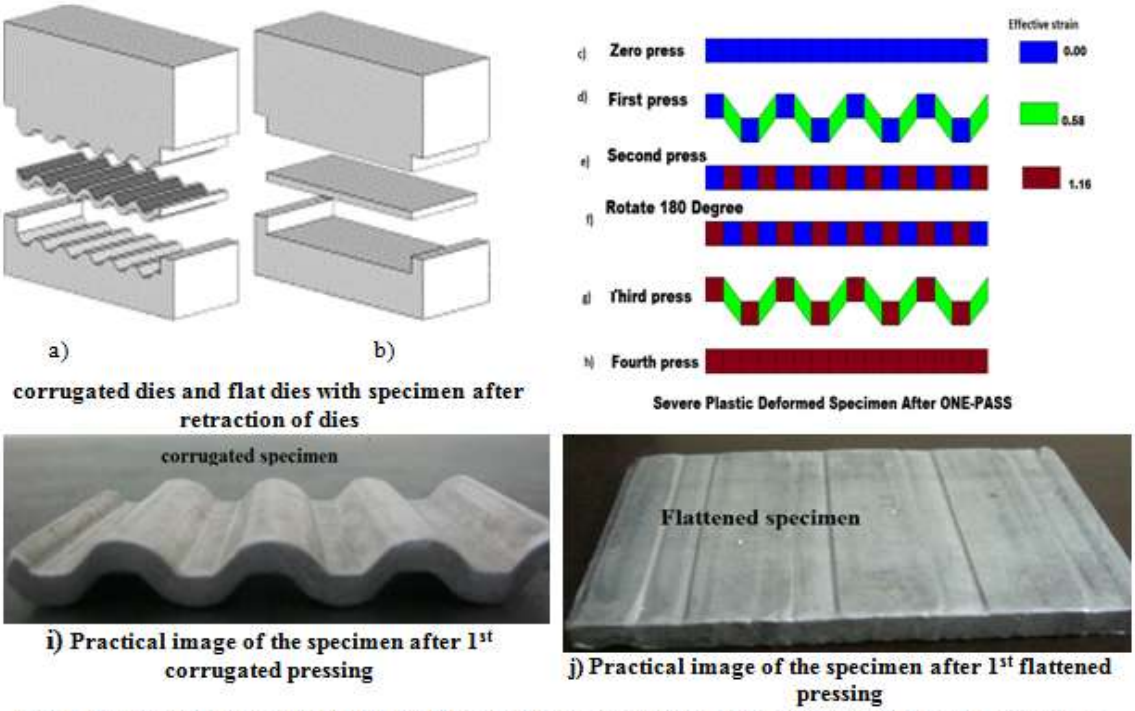


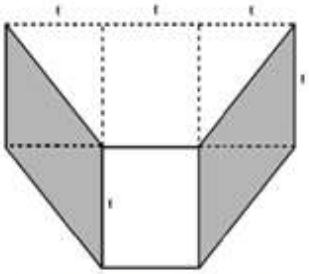
Fig. 2 Schematic of CGP dies (a-b), CGP process stages (c-h) schematic illustration of a CGP technique, and practically processed Al sheets (i-j)

This method comprises bending of a straight plate with corrugated tools and then restoring the straight shape of the plate with flat tools. The repetition of the process is required to obtain a large strain and desired structural changes. It has been shown that ultrafine grained structure can be introduced into metals and alloys via severe plastic deformation. Using CGP method, the coarse grains in pure metals and alloys were successfully refined to the grain size of tens to a few hundreds of nanometers. The submicron grain materials showed very high strength compared to materials with micrometer grain structures. The drawback of ultrafine grained structure materials is their elongation to fracture. Because of low strain hardening in submicron grain structure, the elongation is then dramatically decreased [7–9].Unlike the widely used ECAP process for structure refinement, the CGP process has the advantage that severe plastic deformation can be applied to metal in sheet or plate form[10].The groove pressing is carried out so that the dimension of the gap between the upper die and lower die is the same as the sample thickness and therefore the inclined region of the sample is subjected to theoretically pure shear deformation under plane strain deformation condition. If dies are designed with the groove flank angle (θ) of 45◦, a single pressing yields a shear strain of about 1 in the deformed region. This is equivalent to an effective true strain of 0.58.By repeating this process; a very large amount of plastic strain can be accumulated in the sample without changing its initial dimensions very substantially. The method has been found to have the potential to produce ultrafine structure in plate shape materials. This investigation is an attempt to refine rather coarse grain structure of commercial purity aluminum using CGP technique. The effectiveness of two steps successive groove and flat pressing (corrugation process) was examined with the aim to study the effect of pressing condition on the mechanical behavior of aluminum. The evolution processes of finegrained structure, grain boundary formation and mechanical characteristics developed due to straining process were investigated.

A Pressing sequence schematic illustration of a CGP process is presented in Fig. 2(a-h). At first, a set of asymmetrically grooved dies tightly constrained by groove is prepared. As groove pressing is carried out such that a gap between the upper die and the lower die is same with the sample thickness, the inclined region of the sample (light green shaded area in Fig. 2(d) is subjected to pure shear deformation under plane strain deformation condition. However, no deformation is induced in the flat region (blue shaded area in Fig. 2(d). For the present die design with the groove angle (θ) of 45°, a single pressing yields a shear strain of 1 at deformed region. This is equivalent to an effective strain, €eff of 0.58. The second pressing is performed with a set of flat dies (Fig. 2(b)). By flat pressing under the constrained condition, the previous deformed region is subjected to the reverse shear deformation while the previous unreformed region remains unreformed. The cumulative strain, €eff in the deformed region following the second pressing becomes 1.16 (grey shaded area in Fig. 2(e). After the second pressing, the sample is rotated by 180° (Fig. 2(f)). This allows the undeformed region to be deformed by further pressings due to the asymmetry of the grooved die. Then, the successive pressings with a grooved die (Fig. 2(g)) and a flat die (Fig. 2(h)) result in a homogeneous effective strain of 1.16 throughout the sample. By repeating a CGP process, very large amount of plastic strain can be accumulated in the sample without changing its initial dimensions and, resultantly, an ultra fine grained structure can be obtained. From Fig.2(c,d,e,f,h) are showing flattened CGP specimen , Fig. 2(d and g) are showing corrugated the CGP specimen and Fig. 2(c, d, f, g,h) shows one complete deformation of the plate conducted ,which is equivalent to two pressing and two straitening steps is known as one pass.Fig.2(i and j) shows the Practical image of corrugated and flattened specimen.

3.1 Experimental Procedures

Commercial purity aluminum was supplied in the form of cold-rolled 10 mm thick plate. Prior to CGP pressing, the plate was annealed at the temperature of 250^0C for 1.5 h in order to obtain the recrystallized structure. In the present study, a plate of aluminum with dimensions of 80 × 50 × 5mm was pressed with the CGP technique.



a) Schematic diagram of deformed region in single pressing.

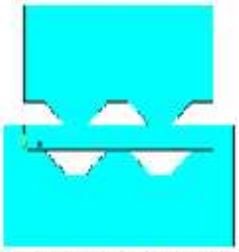
Calculation for Effective strain in the deformed region in a single pressing

$$\gamma = \gamma_{xy} = \frac{x}{t} = \frac{t}{t} = 1 \quad \text{------ (1)}$$

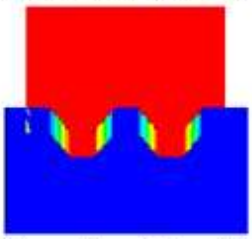
$$\varepsilon_{eff} = \sqrt{\frac{2}{9}\left[(\varepsilon_x - \varepsilon_y)^2 + (\varepsilon_y - \varepsilon_z)^2 + (\varepsilon_z - \varepsilon_x)^2\right] + \frac{4}{3}\left[\varepsilon_{xy}^2 + \varepsilon_{yz}^2 + \varepsilon_{zx}^2\right]} \quad \text{---(2)}$$

$$\varepsilon_{xy} = \frac{\gamma_{xy}}{2} = \frac{\gamma}{2} \quad \text{----(3)} \qquad \varepsilon_x = \varepsilon_y = \varepsilon_z = \varepsilon_{yz} = \varepsilon_{zx} = 0 \quad \text{------(4)}$$

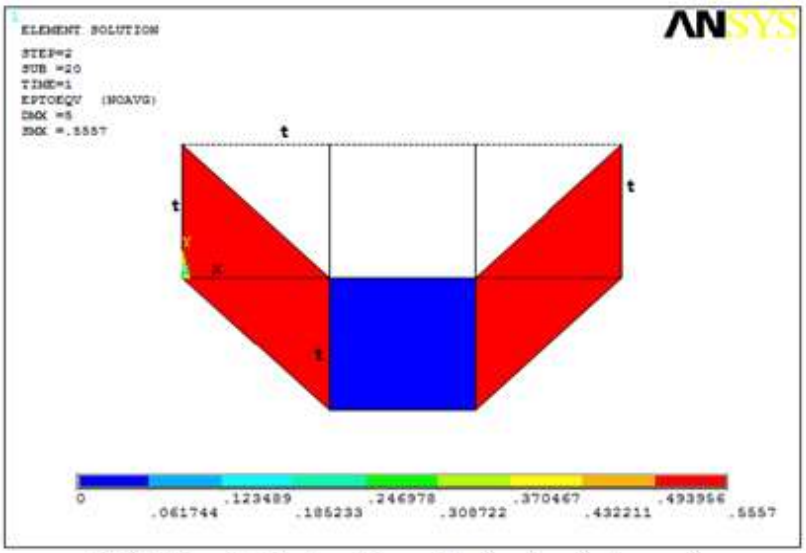
$$(2),(3),(4) \Rightarrow \varepsilon_{eff} = \sqrt{\frac{4(\gamma/2)^2}{3}} \quad \text{----(5)} \qquad \varepsilon_{eff} = \frac{\gamma}{\sqrt{3}} \overset{\gamma=1}{\Rightarrow} \varepsilon_{eff} = 0.58 \quad \text{---(6)}$$



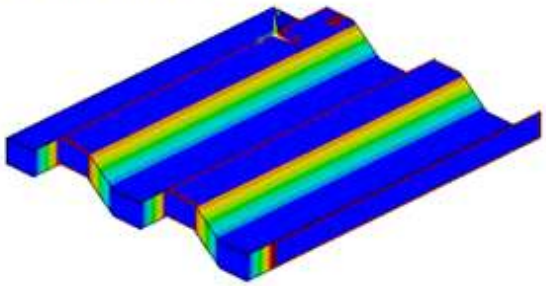
b) Assembly of dies with specimen before pressing



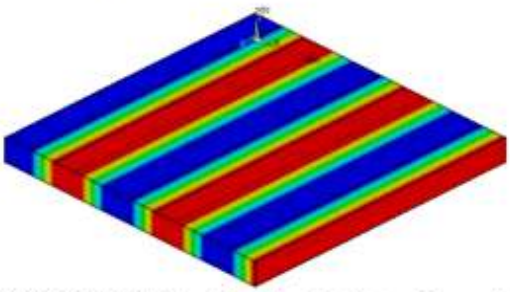
c) Assembly of dies with specimen after pressing



d) Effective strain in the deformed region in a single pressing using ANSYS



(e) 3D-CAD/CAE model After first corrugated press the effective strain in pure shear region are 0.58.



(f) 3D-CAD/CAE model After first flattened press the effective strain in pure shear region are 1.16

Fig.3 (a-f) the scheme of the deformed region in the groove pressed sample with effective strain calculations and 2D&3D -simulation using ANSYS.

In this experiments each process is consists four stages. (1) Flat sheet become corrugated which is results in a 0.58 strain in deformed section (Fig.2(d)). (2) A pair of flat dies flatten the corrugated sheet imposing an extra 0.58 strain to the previously deformed section (Fig.2 (d-e)) it is worth to note that in this stage the sheet has two

different sections; (a) Unstrained section with zero strain.(b) shear strained section with 1.16 strain. (3) the flat sheet is rotated 180^0 around the axis perpendicular to the plane of the sheet and then the stage (1) is repeated. (4) Corrugated sheet is flattened at the end of the 4^{th} pressing the sheet under goes uniform strain magnitude of 1.16 and one pass of CGP accomplished. By repeating the CGP process, a large amount of plastic strain can be accumulated in the work piece without changing its initial dimensions.Referring to fig.3 (a) and Equation (1)-(6),it can be observed that the applied effective strain in the deformed areas in single pressing is equal to 0.58. In this paper to get clear picture of the constrained groove pressing and showing the effective strain calculation through 2D&3D -simulation using ANSYS as shown in the fig.3 (b-f).

3.2 Finite Element Simulation Procedure

In order to investigate the strain distribution in the CGP process after four pressing steps, the finite element technique was accomplished. To investigate the plastic deformation and strain localization behavior of the CGP process, the Elasto-plastic FEM technique was adopted. The simulations were investigated after one full pass using the commercial finite element code ABAQUS/Explicit. The simulation was considered under 2D plane strain condition. Stress–strain curve of the aluminum which was used in the simulations is shown in Fig .4. The kind of mesh used in the simulation is CPE4 elements for the 2D plane strain conditions. The coefficient of friction in the work piece die interface was selected as 0.1, which is within a typical (0.05–0.1) range in the cold forming of metals.

There have been a couple of previous investigations addressing the numerical analysis of the deformation behavior in CGP process [12, 13, 14, 20]. Park and his colleagues simulated the CGP process using FEM, but did not discuss strain and stress distributions in detail. In the present study, the plastic deformation behavior of the specimen during groove pressing was simulated for one full pass using the commercial Elasto-plastic finite element analysis code ABAQUS/Explicit [21]**.** An isothermal two-dimensional plane-strain problem was considered, since deformation along the normal direction is negligible. The number of initial four node iso-parametric plane-strain elements is 497 and nodes 576. This number of elements was found to be sufficient to show the local deformation of the strain rate insensitive materials. The specimen with dimensions of 80 mm in length and 5mm in thickness was considered for simulations (width is unity along the plane normal direction in plane-strain condition). The specimen was modeled with CPE4 mesh and dies were modeled with analytical rigid lines. Pure aluminum material properties were used in all FE simulations.

IV. RESULTS AND DISCUSSIONS

4.1 Micro Hardness

The mean value of hardness as a function of the number of passes for the transverse and perpendicular cross section of the samples is shown in Fig.5. The initial annealed sample had an average hardness of 29 VHN.While after 20 groove pressing (€eff =5.22) it rises to about 55 VHN. Fig.5 shows the hardness variation across the length of the perpendicular cross section of the specimen for each pass. In order to monitor the effect of CGP on the hardening behavior and mechanical homogeneity of the CGPed specimens, the hardness was measured. The receive samples had a mean hardness value of 29 VHN, which increased rapidly to42 VHN after the first pass (€eff=2.32) as a result of strain hardening. After the second (€eff = 2.32), third (€eff = 3.48) passes and after fourth (€eff = 4.64) pass the hardness value increased slightly and then decreased to 49VHN after fifth pass

(Ɛeff = 5.22) . the hardness measured along the center line of the transverse cross section did not vary significatintly,which confirms that the deformation is homogenous along this direction.

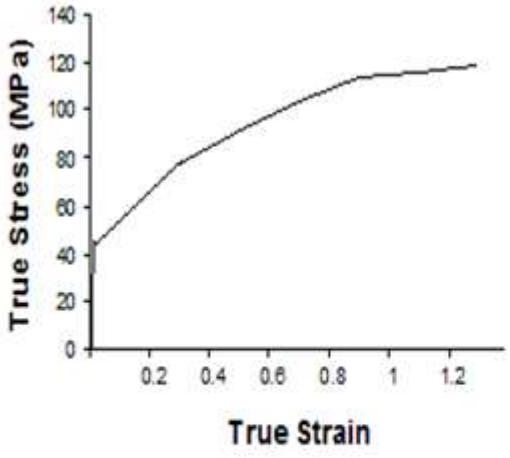


Fig.4. the stress-strain curve of the commercial pure Al used in the Finite element simulations

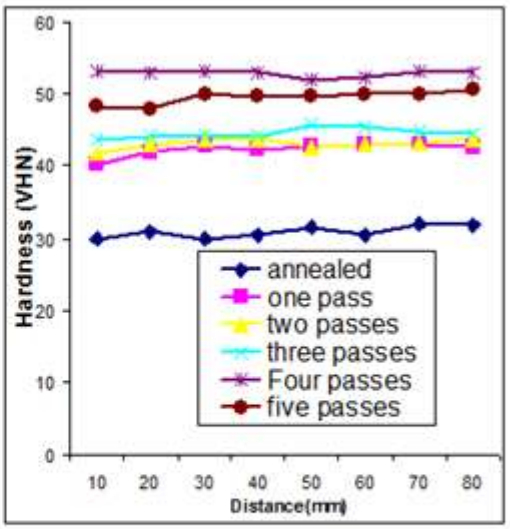


Fig.5. the Vickers hardness variations across the length of the perpendicular cross-section of the specimen for each pass.

5.2 Simulation Results

The distribution of the equivalent plastic strain (PEEQ) in different pressing steps of CGP process in plain strain condition is presented in Fig.6(a-b) (Result of plain stress condition is very similar to plain strain).Variation of PEEQ in the center line of the work piece after the fourth pressing step (one full pass) is presented in Fig 6. The distribution of strain is not uniform and is lower in the surface and interface areas between shear and flat areas (areas near the teeth of the die).

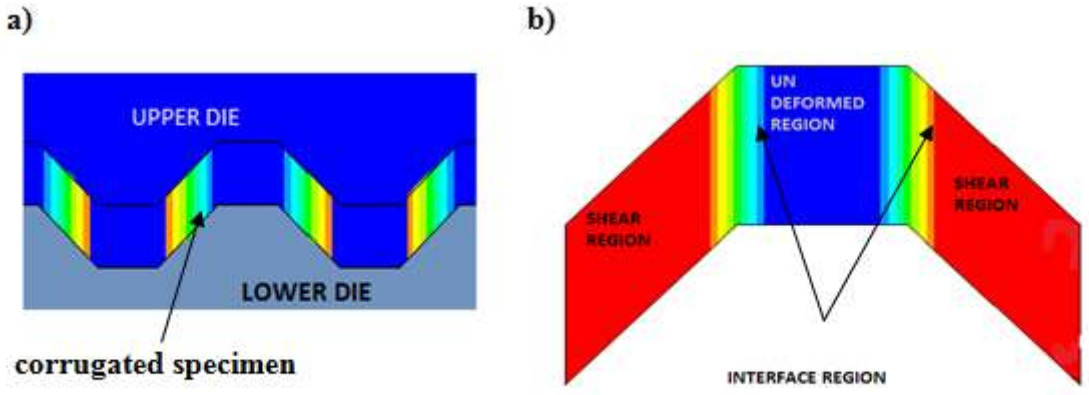


Fig. 6 (A-B) Schematic of Groove Pressing Showing Different Deformation Regions in the Specimen

The specimen was subdivided into three regions according to the deformation modes see Fig.6(b). Shear region, undeformed flat region and interface region between the shear and flat regions. Plastic deformation occurs mainly in the shear region, where the theoretical Von Mises equivalent strain per pressing is 0.58, assuming the deformation mode is simple shear (not pure shear!) and there is no interaction between shear region and flat

regions. Fig.6 shows the variation of Von Mises equivalent strain distributions in CGP processed specimen after two cycles. The strain level increased with the number of passes.

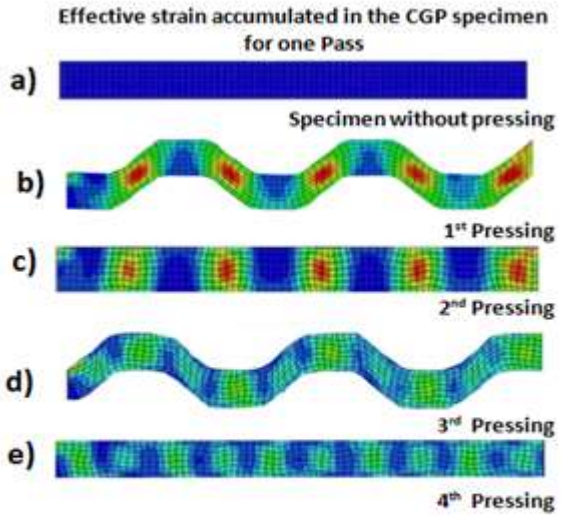


Fig.7 (a-e) Effective strain accumulated in the CGP specimen for one pass

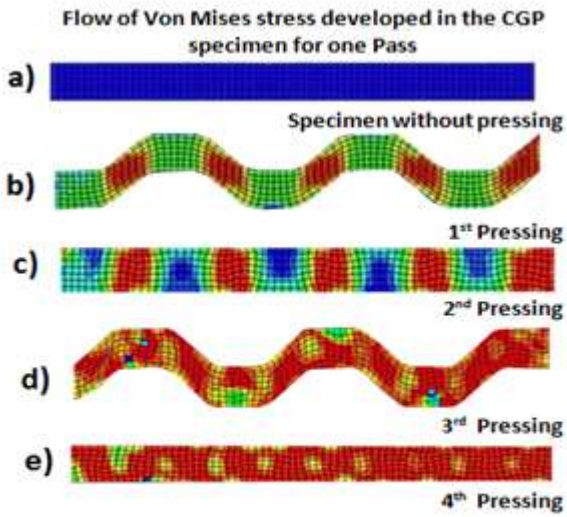


Fig.8 (a-e) Flow of Von Mises stress developed in the CGP specimen for one pass

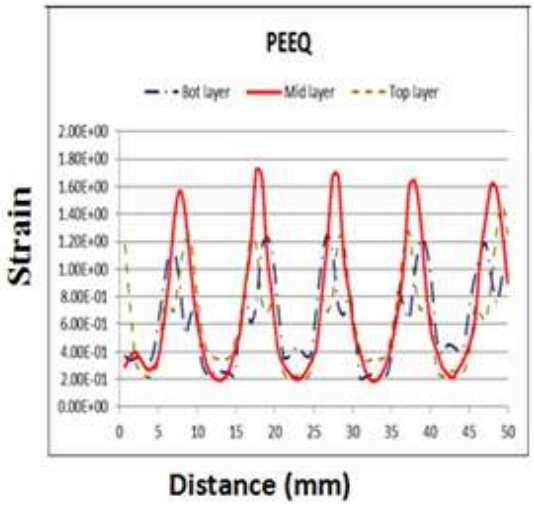
From Fig .7(a-e), it is observed that the in homogeneity within the specimen was higher as the number of cycles increased. Looking at the first cycle, the Von Mises equivalent strain ε_{eff} values after first pressing and first flattening in the first shear region are $\varepsilon_{eff} = 0.80$ and $\varepsilon_{eff} = 1.66$, respectively, which are larger than theoretical values $\varepsilon_{eff} = 0.58$ and $\varepsilon_{eff} = 1.16$ of the simple shear during the first cycle. This is because of the interaction between the shear region and flat region: more deformation is generated in the shear region in CGP than in the region of simple shear alone. Because of the interaction between the shear region and flat region, the deformation mode in CGP is not simple shear.

The flat regions deform by a negligible amount of deformation during the pressing and flattening steps. During the flattening steps, the flat regions do not deform but the shear regions deform by the same amount of shear strain in the reverse direction. The top die was shifted in the simulation towards RHS(or the specimen rotated about 1800 in the plane of pressing) by the width of the flat regions (that of the shear region 5 mm), between the first flattening and the second pressing steps, in order to impose deformation in the previously undeformed flat regions after first pressing (undeformed regions). It can be found that, the deformation obtained in the first cycle was a little more homogeneous after second flattening than after the first flattening. Even though strain localization was relieved after the second cycle, compared to the first cycle, strain is not as homogeneous as expected. The strain between the maximum and minimum points after the second flattening was smaller than that in the first flattening due to the differences in the relative strength of the flat regions surrounding the shear regions. During the first pressing and flattening steps the relative strength of the flat regions surrounding the shearing region is weak, and deformation diffuses out of the shear region. For the second cycle, the situation of strain localization does not change. The differences in strain between the maximum and minimum points after first flattening and the second flattening are 1.68 and 1.66, respectively. It should be noted that strain distribution after the second flattening is a little more homogeneous than that after the first flattening.

Fig.7(a,b,c,d,e) shows the unreformed specimen , the Deformation of specimen in First corrugated pressing the strain is developed, the Deformation of specimen in First flattened pressing the strain is developed , After 1800 rotation of the first flattened specimen ,the Deformation of specimen in Second corrugated pressing the strain is developed, the Deformation of specimen in Second flattened pressing the strain is developed. Effective strain accumulated in the CGP specimen for one pass (Four pressing) shown in Fig.7 (a-e) Similarly Flow of Von Mises stress developed in the CGP specimen for one pass shown in Fig.8(a-e).

Fig.9 & Fig.10 shows the effective strain distribution in different layers in CGP specimen, i.e Bottom layer, Middle layer and Top layer. From Fig.9 it shows the strain uniformly distribute in the middle layer strain is 1.68 but in top and bottom layer, strain distribution is less in first straightening. From Fig.10 it shows the strain uniformly distribute in the middle layer, strain is about 2.5 but in top and bottom layer strain distribution is less in second straightening process.

Although the average strain level increases, the strain localization intensified with increasing number of CGP cycles, stress need not always follow the same trend, because the stress gradient decreases with strain. It is evident that the stress distribution can be considered as relatively uniform, compared to the strain distribution. The experimental stress values estimated from the hardness are in reasonably good agreement with the simulated results.



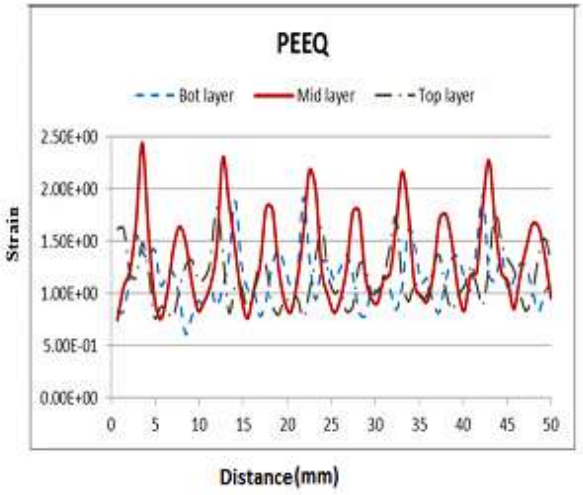


Fig.9 Equivalent Strain after First Straightening **Fig.10 Equivalent Strain after second Straightening**

VI. CONCLUSION

- In this study the complete simulation of two corrugation and two straitening process is made using CAD/CAE tools. The commercial pure aluminum CGPed samples were pressed up to five passes.
- From the previous literatures and studies, nanostructured material can be produced by Severe Plastic Deformation (SPD) methods, from these studies it was noted that the CGP method is the most applicable for producing Nanostructured sheet metals.
- The CGP process produces high quality nanostructured materials, where, the quality of surface roughness improves with the increasing number of passes. Also, this process concerned with produce metals and alloys with controlled Nano-sized grains, and free from defects such as porosity, cracks, or other atomic scale defects that are known to compromise properties.

- Hardness increased in the first three passes and then trend decreased slightly at the fourth and fifth pass. Greater refinement of aluminium microstructure and further increase in strengths is expected to occur with larger number of executed passes.
- The hardness measured along the central line of the transverse cross-section did not vary significantly but the non-homogeneity is observed in FEA results. The stress distribution can be considered as relatively uniform, compared to the strain distribution.
- The results of 2D plain strain and plain stress condition showed that PEEQ in the inclined shear region is higher than the theoretical value and after four pressing steps PEEQ is not uniform throughout the work piece and is lower in the areas near the surface and the teeth of the grooved die.

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A FOOD RECOGNITION SYSTEM FOR DIABETIC PATIENTS USING SVM CLASSIFIER

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ABSTRACT

Computer vision-based food recognition could be used to estimate a meal's carbohydrate content for diabetic patients. This study proposes a methodology for automatic food recognition, based on the bag-of-features (BoF) model,GLCM and LBP features. Moreover, the enhancement of the visual dataset with more images will improve the classification rates, especially for the classes with high diversity. The final system will additionally include a food segmentation stage before applying the proposed recognition module, so that images with multiple food types can also be addressed. The optimized system computes dense local features, using the scale-invariant feature transform on the HSV color space and texture features and these extracted features are trained and classified using SVM classifier. The system achieved classification accuracy of the order of 90%, thus proving the feasibility of the proposed approach in a very challenging image dataset.

Keywords: Diabetic Patients, Recognition Module, Optimized System, Texture Features

I. INTRODUCTION

The treatment of Type 1 diabetic (T1D) patients involves exogenous insulin administration on a daily basis. A prandial insulin dose is delivered in order to compensate for the effect of a meal [1]. The estimation of the prandial dose is a complex and time-consuming task, dependent on many factors, with carbohydrate (CHO) counting being a key element.Clinical studies have shown that, in children and adolescents on intensive insulin therapy, an inaccuracy of ±10 g in CHO counting does not impair postprandial control [2], while a±20 g variation significantly impacts postprandial glycaemia [3]. There is also evidence that even well-trained T1D patients find it difficult to estimate CHO precisely [4]–[6]. In [4], 184 adult patients on intensive insulin were surveyed with respect to the CHO content of their meals. On average, respondents overestimated the CHO contained in their breakfast by 8.5% and underestimated CHO for lunch by 28%, for dinner by 23%, and for snacks by 5%. In [5], only 23% of adolescent T1D patients estimated daily CHO within 10 g of the true amount, despite the selection of common meals.

The increased number of diabetic patients worldwide, together with their proven inability to assess their diet accurately raised the need to develop systems that will support T1D patients during CHO counting. So far, a broad spectrum of mobile phone applications have been proposed in the literature, ranging from interactive diaries [7] to dietary monitoring based on on-body sensors [8]. The increasing processing power of the mobile devices, as well as the recent advances made in computer vision, permitted the introduction of image/video analysis-based applications for diet management [9]–[14]. In a typical scenario, the user acquires an image of

the upcoming meal using the camera of his phone. The image is processed—either locally or on the server side—in order to extract a series of features describing its visual properties. The extracted features are fed to a classifier to recognize the various food types of the acquired image, which will then be used for the CHO estimation. A food recognition application was introduced by Shroff*et al*. [9] for the classification of fast-food images into four classes. For each segmented food item, a vector of color (normalized RGB values), size, texture (local entropy, standard deviation, range), shape, and context-based features is computed and fed to a feed-forward artificial neural network (ANN), resulting in recognition accuracy of the order of 95%, 80%, 90%, and 90% for hamburgers, fries, chicken nuggets, and apple pies, respectively. A set of color (pixel intensities and color components) and texture (Gabor filter responses) features was used by Zhu *et al*. [10], together with a support vector machine (SVM) classifier, for the recognition of 19 food classes, leading to a recognition rate of the order of 94% for food replicas and 58% for real food items.Kong and Tan [11] proposed the use of scale invariant feature transform (SIFT) features clustered into visual words and fed to a simple Bayesian probabilistic classifier that matches the food items to a food database containing images of fast-food, homemade food, and fruits. A recognition performance of 92% was reported given that the number of references per food class in the database is larger than 50 and the number of food items to be recognized is less than six.

II. RELATED WORK

Puri*et al.* [14] proposed a pairwise classification framework that takes advantage of the user's speech input to enhance the food recognition process. Recognition is based on the combined use of colorneighborhood and maximum response features in a texton histogram model, feature selection using Adaboost, and SVM classifiers. Texton histograms resemble BoF models, using though simpler descriptors, such that histograms of all possible feature vectors can be used. In this way, the feature vector clustering procedure can be omitted; however, less information is considered by the model which might not be able to deal with high visual variation. Moreover, the proposed system requires a colored checker-board captured within the image in order to deal with varying lighting conditions. In an independently collected dataset, the system achieved accuracies from 95% to 80%, as the number of food categories increases from 2 to 20.

A database of fast-food images and videos was created and used by Chen *et al*. [15] for benchmarking of the food recognition problem. Two image description methods were comparatively evaluated based on color histograms and bag of SIFT features for a seven fast-food classes problem. The mean classification accuracy using an SVM classifier was 47% for the color histogram based approach and 56% for the SIFT-based approach. However, the used patches are sampled with the SIFT detector which is generally not a good choice for image classification problems, and described by the standard grayscale SIFT that ignores any color information.

The combined use of bag of SIFT, Gabor filter responses, and color histograms features in a multiple kernel learning (MKL) approach was proposed by Joutou*et al*. [16] for the recognition of Japanese food images. However, the employed BoF model uses the conventional scheme of fixed-size SIFT features clustered with standard *k*-means, while the additional color and texture features are global and are not included into the BoF

architecture. For the 50 food classes problem, a mean recognition rate of 61% was reported. The present study makes several contributions to the field of food recognition. A visual dataset with nearly 5000 homemade food images was created, reflecting the nutritional habits in central Europe [17]. The foods appearing in the images have been organized into 11 classes of high intravariability. Based on the aforementioned dataset, we conducted an extensive investigation for the optimal components and parameters within the BoF architecture.

III. PROPOSED METHOD

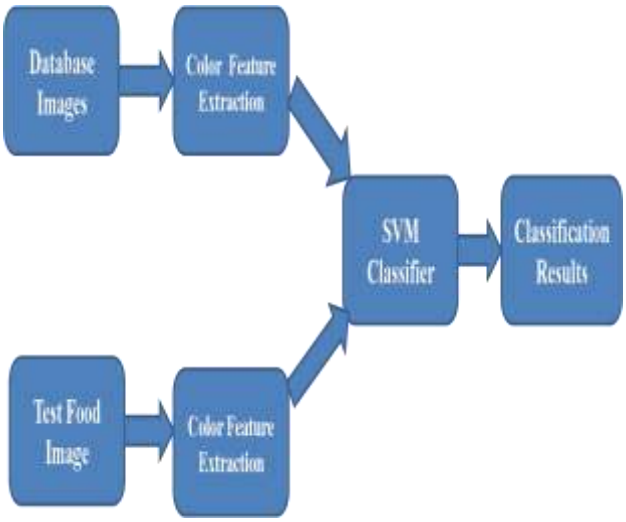

FIG 3.1: Block Diagram

3.1 Food Image Description

In order to describe the appearance of the different food classes, the BoF model was adopted, due to its proven ability to deal with high visual diversity and the absence of typical spatial arrangement within each class. BoF consists of four basic steps: 1) key point extraction, 2) local feature description, 3) learning the visual dictionary, and 4) descriptor quantization. All the steps, as presented in Fig. 1, are involved in both training and testing, except for the learning of the dictionary, which is performed only once, during the training phase. *1) Key Point Extraction:* Key points are selected points on an image that define the centers of local patches where descriptors will be applied. In the current study, three different key point extraction methods were tested: interest point detectors, random sampling, and dense sampling. Interest point detectors, such as SIFT [18], are considered as the best choice for image matching problems where a small number of samples is required, as it provides stability under local and global image perturbations. SIFT estimates the key points by computing the maxima and minima of the difference of Gaussians (DoG), applied at different scales of the image.

3.2 Local Feature Description

After the key point extraction, a local image descriptor is applied to a rectangular area around each key point to produce a feature vector. Identifying the appropriate descriptor size and type for a recognition problem is a challenging task that involves a number of experiments. For the determination of the optimal descriptor size, the size of the object to be recognized should be considered. Although the SIFT interest point detector provides the

position of the key points together with their scale, it is rarely used for image classification, as already explained. Hence, the size of the descriptor must be specified somehow after the dense or random key point sampling. A minimum size of 16 × 16 is often used as proposed in [18], since a smaller patch would not provide sufficient information for the description. However, the use of larger sizes or combination of sizes can often give better results by resembling the multiscale image description of the SIFT detector. It should be noted that food images are scaled to a standard size, so differences in food items scale should not be extreme.

3.3. Color Histograms

Color histograms are probably the most common color descriptors. They represent the color distribution of an image in a certain color space and—despite their simplicity—they have been successfully used in various object recognition applications [20]. For the proposed system, five color histograms were considered covering different combinations of invariants: *HistRGB*, *HistOp*, *HistRG*norm, *HistHue*, *and HistRGB*trans calculated in the RGB color space (1), the opponent color space (2), the RG normalized channels (3), the Hue channel (4), and the transformed RGB color space (5), respectively:

$$\mathrm{RGB} = \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

$$\mathrm{Op} = \begin{pmatrix} O_1 \\ O_2 \\ O_3 \end{pmatrix} = \begin{pmatrix} \frac{R-G}{\sqrt{2}} \\ \frac{R+G-2B}{\sqrt{2}} \\ \frac{R+G+B}{\sqrt{3}} \end{pmatrix}$$

$$\mathrm{RG}_{\mathrm{norm}} = \begin{pmatrix} R_{\mathrm{norm}} \\ G_{\mathrm{norm}} \end{pmatrix} = \begin{pmatrix} \frac{R}{R+G+B} \\ \frac{G}{R+G+B} \end{pmatrix}$$

$$\mathrm{Hue} = \operatorname{atan2}\left(\sqrt{3} * (G-B), 2 * R - G - B\right)$$

$$\mathrm{RGB}_{\mathrm{trans}} = \begin{pmatrix} R_{\mathrm{trans}} \\ G_{\mathrm{trans}} \\ B_{\mathrm{trans}} \end{pmatrix} = \begin{pmatrix} \frac{R-\mu_R}{\sigma_R} \\ \frac{G-\mu_G}{\sigma_G} \\ \frac{B-\mu_B}{\sigma_B} \end{pmatrix}$$

3.4. SVM

SVMs are a set of related supervised learning methods that analyze data and recognize patterns, used for classification and regression analysis. The standard SVM takes a set of input data, and predicts, for each given input, which of two possible classes the input is a member of, which makes the SVM a non-probabilistic binary linear classifier. Since an SVM is a classifier, then given a set of training examples, each marked as belonging to one of two categories, an SVM training algorithm builds a model that predicts whether a new example falls into one category or the other.

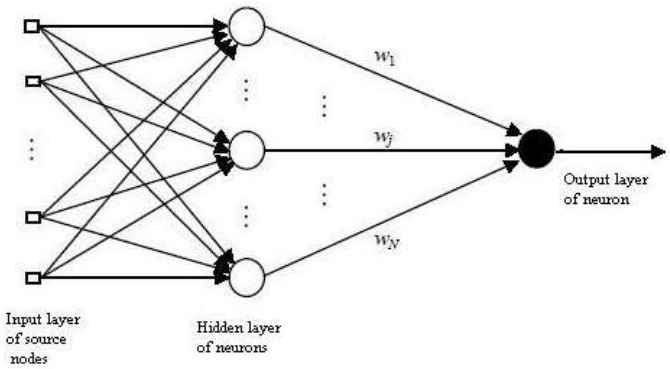

Fig 3.2. Architecture of SVM

Fig. 3.3 (a)-(c) High Calorie food images

Fig 3.3.(a)-(c) Low Calorie food images

IV. SIMULATION RESULT

4.1 High Calorie Food Image

4.1.1 Testing Images

Fig 4.1 Breaded Vegetable

4.2 Local Binary Pattern Features

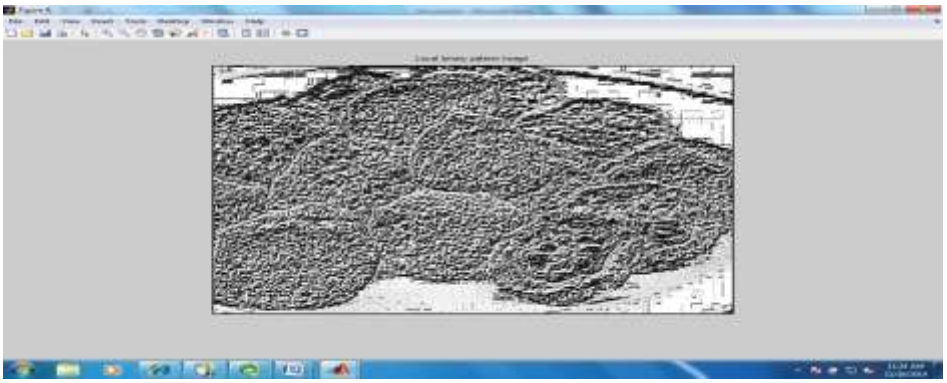

Fig 4.2 Local Binary Pattern

4.3 Gray Level Co-Occrrence Matrix Feature

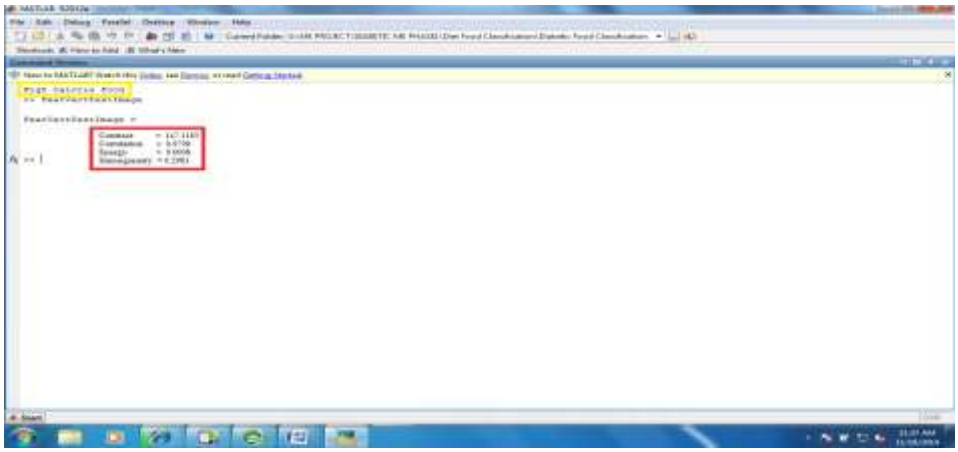

Fig 4.3Graylevel co-occrrence matrix

High Calorie Food

Contrast = 147.1183

Correlation = 0.9709

Energy = 0.0008

Homogeneity = 0.2983

V.CONCLUSION

In this paper, we propose a BoF-based system for food image classification, as a first step toward the development of a portable application, providing dietary advice to diabetic patients through automatic CHO counting. The final system will additionally include a food segmentation stage before applying the proposed recognition module, so that images with multiple food types can also be addressed.

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FPGA IMPLEMENTATION OF BILATERALFILTER AND OPTIMAL PARAMETER ESTIMATION FOR IMAGE DENOISING

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ABSTRACT

An image is often corrupted by noise in its acquisition or transmission. The goal of denoising is to remove the noise while retaining as much as possible the important signal features. The bilateral filter is a local non-linear filter, that's response depends on both gray level similarities and geometric closeness of the neighboring pixels without smoothing edges. The filter's neighbor pixel size and width (sigma) determines efficiency of the filter. Hence, an important issue with the application of the bilateral filter is the selection of the filter parameters, which affect the results significantly. We propose particle neighbor scale and filter's widths for spatial and Intensity of the bilateral filter extracted from scaled image.

Keywords: Image Noises , Bilateral Filter, Image Restoration.

I. INTRODUCTION

An image is a visual representation of an object, a person, or a scene produced by an optical device such as a mirror, a lens, or a camera. This representation is two dimensional (2D), although it corresponds to one of the infinitely many projections of a real-world, three-dimensional (3D) object or scene. A digital image is a representation of a two-dimensional image using a finite number of points, usually referred to as picture elements, pels, or pixels. Each pixel is represented by one or more numerical values: for monochrome (grayscale) images, a single value representing the intensity of the pixel (usually in a [0, 255] range) is enough; for color images, three values (e.g., representing the amount of red (R), green (G), and blue (B)) are usually required.

Binary images are the simplest type of images and can take only two discrete values, black and white. Black is represented with the value '0' while white with '1'. Note that a binary image is generally created from a gray-scale image. A binary image finds applications in computer vision areas where the general shape or outline information of the image is needed. They are also referred to as 1 bit/pixel images. Gray-scale images are known as monochrome or one-color images. The images used for experimentation purposes in this thesis are all gray-scale images. They contain no colour information. They represent the brightness of the image. This image contains 8 bits/pixel data, which means it can have up to 256 (0-255) different brightness levels.

A '0' represents black and '255' denotes white. In between values from 1 to 254 represent the different gray levels. As they contain the intensity information, they are also referred to as intensity images. Color images are considered as three band monochrome images, where each band is of a different color. Each band provides the

brightness information of the corresponding spectral band. Typical color images are red, green and blue images and are also referred to as RGB images. This is a 24 bits/pixel image.

II. IMAGE NOISES

A very large portion of digital image processing is devoted to image restoration. This includes research in algorithm development and routine goal oriented image processing. Image restoration is the removal or reduction of degradations that are incurred while the image is being obtained Degradation comes from blurring as well as noise due to electronic and photometric sources. Blurring is a form of bandwidth reduction of the image caused by the imperfect image formation process such as relative motion between the camera and the original scene or by an optical system that is out of focus. When aerial photographs are produced for remote sensing purposes, blurs are introduced by atmospheric turbulence, aberrations in the optical system and relative motion between camera and ground. In addition to these blurring effects, the recorded image is corrupted by noises too. A noise is introduced in the transmission medium due to a noisy channel, errors during the measurement process and during quantization of the data for digital storage. Each element in the imaging chain such as lenses, film, digitizer, etc. contribute to the degradation.

Image denoising is often used in the field of photography or publishing where an image was somehow degraded but needs to be improved before it can be printed. For this type of application we need to know something about the degradation process in order to develop a model for it. When we have a model for the degradation process, the inverse process can be applied to the image to restore it back to the original form. This type of image restoration is often used in space exploration to help eliminate artifacts generated by mechanical jitter in a spacecraft or to compensate for distortion in the optical system of a telescope. Image denoising finds applications in fields such as astronomy where the resolution limitations are severe, in medical imaging where the physical requirements for high quality imaging are needed for analyzing images of unique events, and in forensic science where potentially useful photographic evidence is sometimes of extremely bad quality.

III. RELATED WORK

T. Q. Vinh, J. H. Park, Y.-C.Kim, and S. H. Hong have proposed “FPGA Design And Implementation Of A Wavelet-Domain Video Denoising System”Multiresolution video denoising is becoming an increasingly popular research topic over recent years. Although several wavelet based algorithms reportedly outperform classical single-resolution approaches, their concepts are often considered as prohibitive for real-time processing. Little research has been done so far towards hardware customization of wavelet domain video denoising. A number of recent works have addressed the implementation of critically sampled orthogonal wavelet transforms and the related image compression schemes in Field Programmable Gate Arrays (FPGA). However, the existing literature on FPGA implementations of over complete (non-decimated) wavelet transforms and on manipulations of the wavelet coefficients that are more complex than thresholding is very limited. In this paper we develop FPGA implementation of an advanced wavelet domain noise interring algorithm, which uses a non-decimated wavelet transform and spatially adaptive Bayesian wavelet shrinkage.

The standard composite television video stream is digitalized and used as source for real-time video sequences. The results demonstrate the e effectiveness of the developed scheme for real time video processing.

F.Hannighave proposed "A DeeplyPipelined and Parallel Architecture For Denoising Medical Images"

the filter consists of 16 parallel working modules, where the most computationally intensive module achieves software pipelining of a factor of 85, that is, computations of 85 iterations overlap each other. By applying a state-of-the-art high-level synthesis tool, we show that this approach can be used for real world applications. In addition, we show that our high level synthesis tool is capable of significantly reducing the well-known productivity gap of embedded system design by almost two orders of magnitude. Finally, we can conclude that the FPGA implementation of the multiresolution image processing algorithm is far ahead of a comparable implementation for graphics cards in terms of power efficiency. Multiresolution video denoising is becoming an increasingly popular research topic over recent years. Although several wavelet based algorithms reportedly outperform classical single-resolution approaches, their concepts are often considered as prohibitive for real-time processing.However, the existing literature on FPGA implementations of overcomplete (non-decimated) wavelet transforms and on manipulations of the wavelet coefficients that are more complex than thresholding is very limited. In this paper we develop FPGA implementation of an advanced wavelet domain noise itering algorithm, which uses a non-decimated wavelet transform and spatially adaptive Bayesian wavelet shrinkage. The standard composite television video stream is digitalized and used as source for real-time video sequences. The results demonstrate the e effectiveness of the developed scheme for real time video processing.

Gabiger-Rose, M. Kube, P. Schmitt, R. Weigel, and R. Rose have developed"Medical Image DenoisingOn Field Programmable Gate Array Using Finite RandomTransform"This study presents the design and implementation of efficient architectures for finite Radon transform (FRAT) on a field programmable gate array (FPGA). FPGA-based architectures with two design strategies have been proposed: direct implementation of pseudo-code with a sequential or pipelined description, and a block random access memory-based approach. Various medical images modalities have been deployed for both software evaluation and hardware implementation. Xilinx DSP tool has been used to improve the implementation time and reduce the design cycle and the Xilinx software has been used for generating a hardware description language from a high-level MATLAB description. Objective evaluation of image denoising using FRAT is carried out and demonstrates promising results. Moreover, the impact of different block sizes on image reconstruction has been analysed. Performance analysis in terms of area, maximum frequency and throughput is presented and reveals significant achievements.

B. K. Shreyamsha Kumar have proposed "Image Denoising By Thresholding In The Wavelet Domain And Implementation In FPGA Using VHDL"HereWavelet transform has the advantage of visualizing the parameter both in Time and Frequency Domain this technique has been effective in noise removal with minimum side effects on important features such as image details and edges. It gives VLSI architecture implementation in FPGA for image processing. The image decomposed into L levels and the detail and approximation coefficients are found and the denoising using Hard and Soft thresholding is applied and the denoised coefficients are reconstructed to get the denoised image. Efficient hardware implementation based on FPGA technology is

proposed.The image processing toolbox [Im01] in Matlab provides the medfilt2() [Appendix] function to do median filtering on an image. The input image and the size of the window are the parameters the function takes.

IV. PROPOSED WORK

Denoising has long been a focus of research and yet there always remains room for improvement, especially in image denoising. The simple spatial filtering of a corrupted image can be successful when high frequency noise is to be removed from the corrupted image. The main difficulty associated with this is, the computational complexity involved in performing the convolution.The goal of image denoising is to remove the noise while retaining the important image features like edges, details as much as possible. Linear filters, which consist of convolving the image with a constant matrix to obtain a linear combination of neighborhood values, have been widely used for noise elimination in the presence of additive noise. Bilateral Filter proposed in considers both spatial and intensity information between a point and its neighboring points, unlike the conventional linear filtering where only spatial information is considered. This preserves the edges/sharp boundaries very well while noise is averaged out as it average pixels belonging to the same region as the reference pixel.Thedenoising performance of bilateral depends on gaussian filter coefficient. The Gaussian filter designed with tow parameters neighboring window size and sigma value of filters. The adaptive changing the parameters give better denoising results as well as fast of completion of denoising process. The proposed bilateral filter perfume better denoising process over existing method of bilateral filter comparison done by quality of denoised image in terms of psnr (peak signaltonoise radio) and mse (mean square error) value.The both filter sigma value estimated adaptively from local region of image The sigma value of the bilateral filter is estimated from Z-score value of local neighborhood pixels.

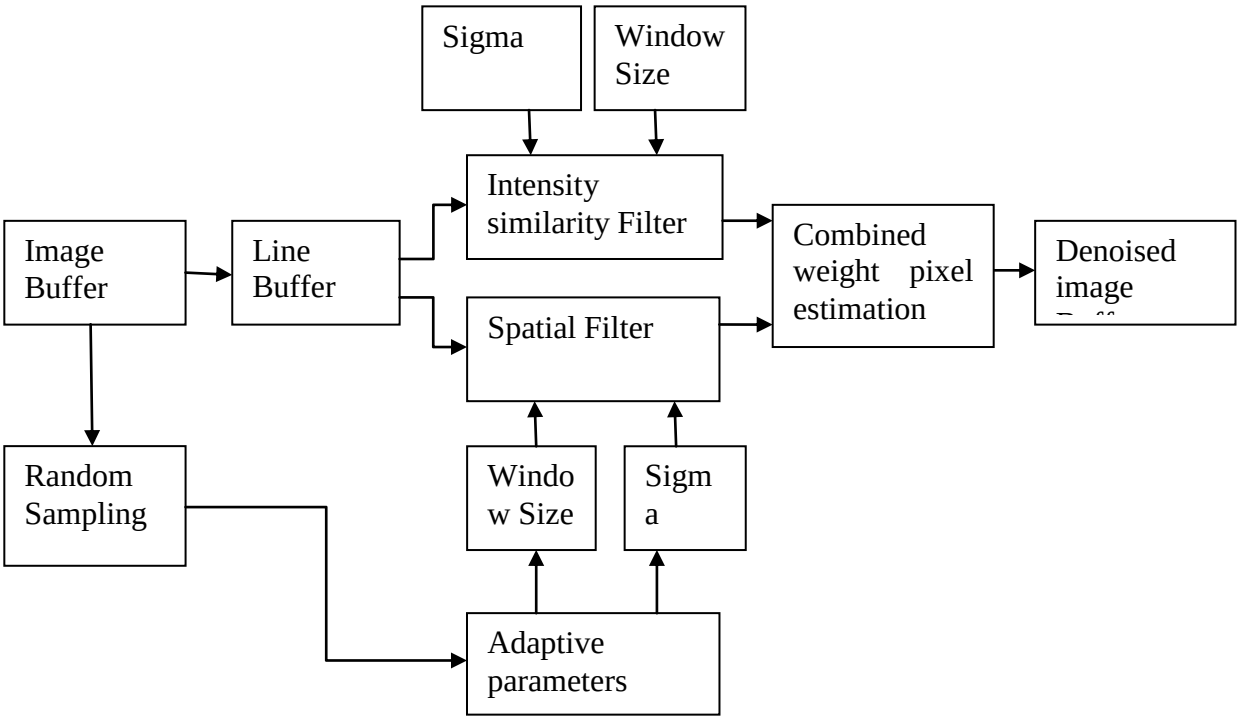

Fig 4.1 Block Diagram

V. SIMULATION RESULT

To open the Xilinx ISE 10.1, click on the Xilinx icon 

on the desk top or go to the **Start -> Programs -> Xilinx ISE Design Suit 10.1 -> ISE -> Project Navigator**

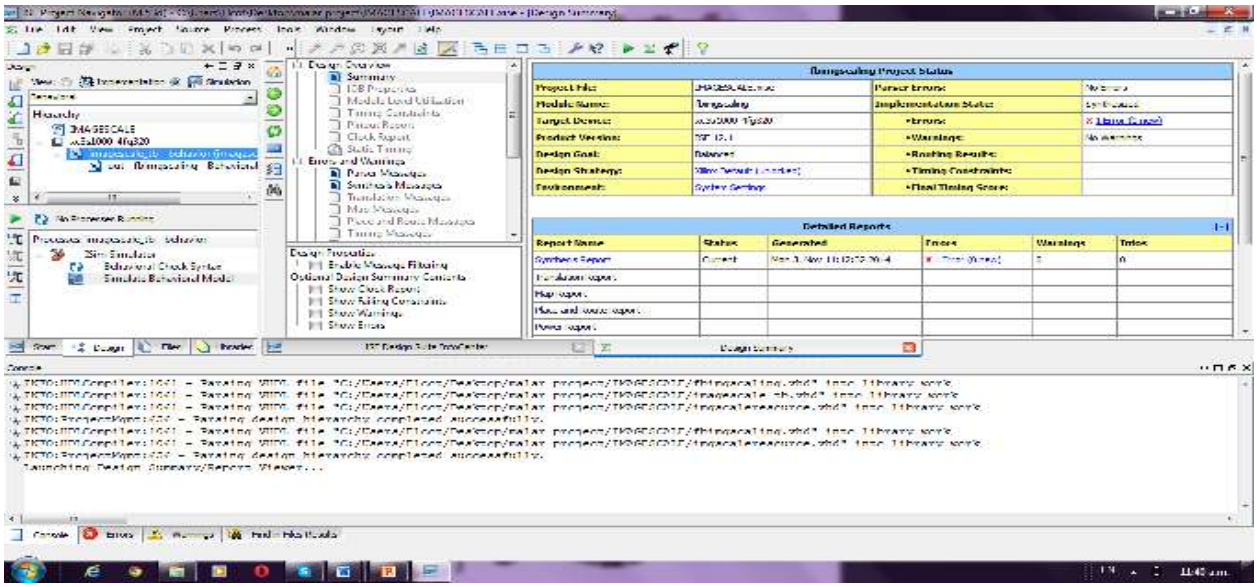

Fig 5.1Starting Window

To create the process and write the code for producing the output

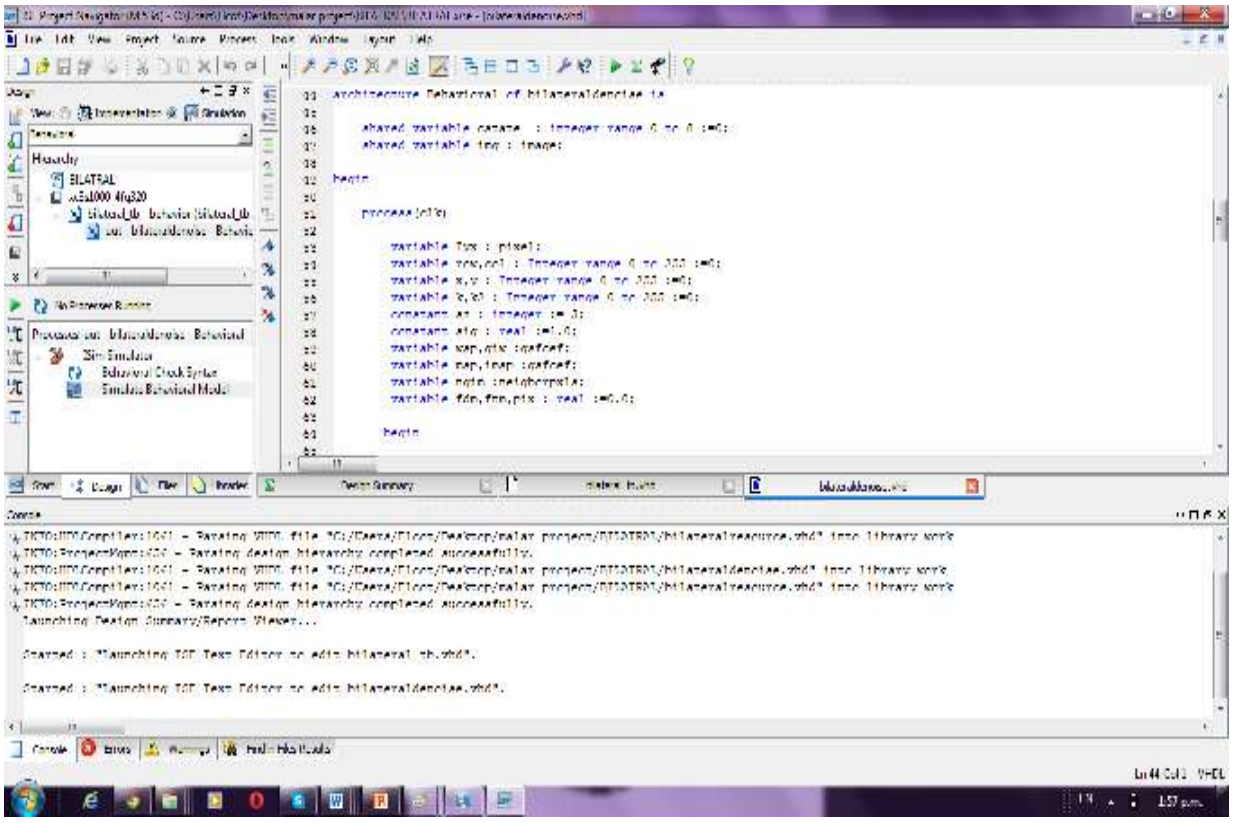

Fig 5.2Processing Window

Output waveform

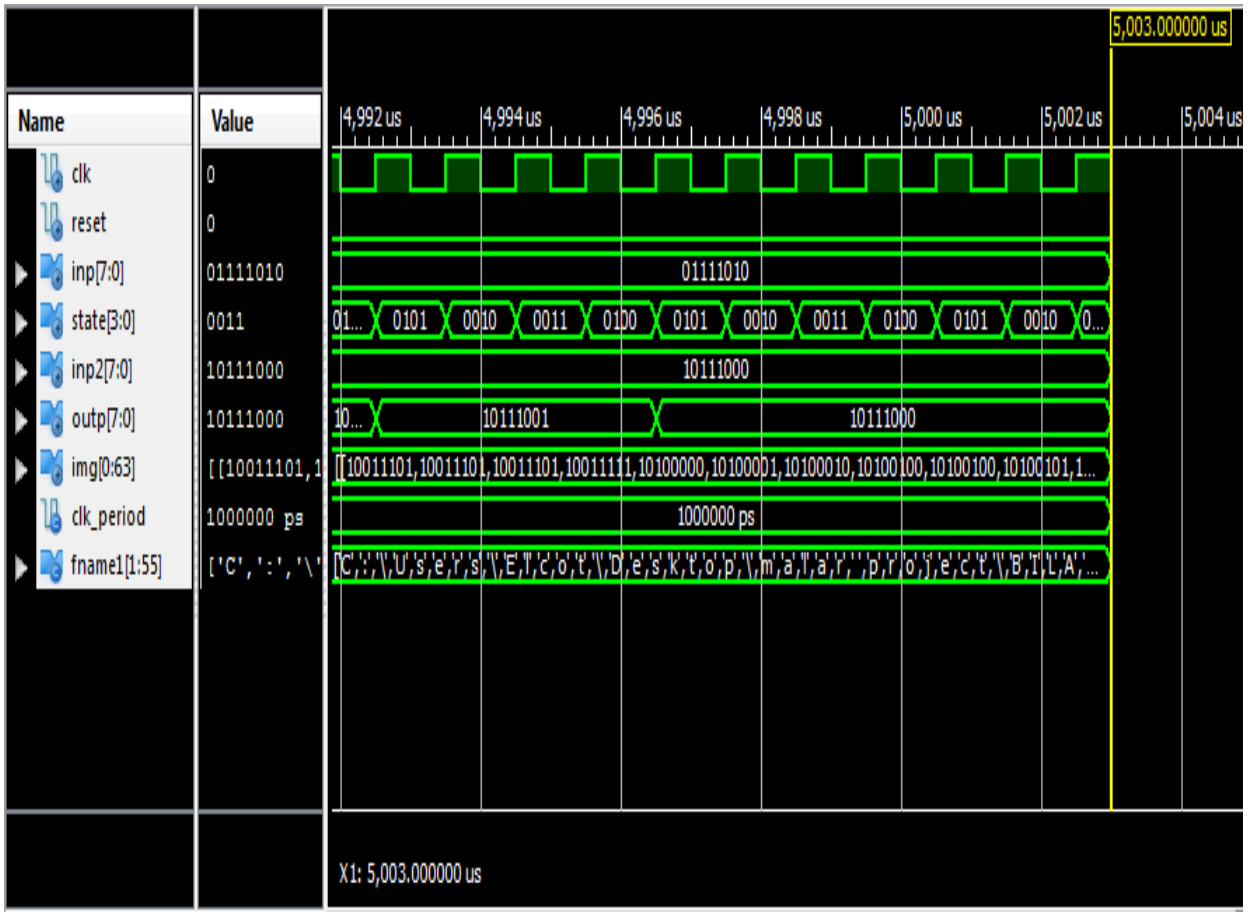

Fig 5.3 Output Waveform for Denoised Image

VI. CONCLUSION

Bilateral filter for image adaptive denoising process in FPGA using vhdl hardware language. The image denoising performance of bilateral improved by adaptively determining filter parameters (size and sigma) instead of fixed filter's size and sigma. The adaptive changing the parameters give better denoising results as well as fast of completion of denoising process than fixed filter model. The denoised Image quality was assessed with PSNR (peak signal to noise ratio) and MSE (mean square value) value.

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DESIGN AND ANALYSIS FOR REGENERATING THE ENERGY FROM BUILDING LIFT

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ABSTRACT

The intention of this specification is to set out the standard of require for lift installations. All lifts shall be robust, reliable and shall meet the department users' requirements and expectations. Lift installation must comply with all current regulations, including Building Regulations. The appointed Design Consultant will be responsible for traffic analysis to provide the most suitable lift solution, including items such as size of lift car, contract load, type of load and its associated safety features, speed, number of passengers etc. Major Modernization is a reasonably straight forward exercise in that, with the exception. It may be possible to increase the lift speed which would reduce travel time between floors. However, this is govern by strict lift regulations and is only possible where the clear headroom at the top of the lift well and the pit depth at the bottom of the lift well are sufficient to allow this. The clauses in this part of the Specification cover all items which are generally standard in this type of installation, while the Particular specification covers the materials and method to be used in the Works.

The following clauses apply equally to new lift installations, major modernization and refurbishments. Where existing installations do not comply with these standards they shall be brought up to date as far as is reasonably practicable. Any remaining sections of the existing installations that do not comply with this specification shall be highlighted and drawn to the attention. In the existing system the new design is used for converting unutilized mechanical energy into electrical energy and it is compactly fitted into headroom. This new design is specific to the regenerate the electrical energy from mechanical energy of the lift which is stored in battery and it will use whenever the light is off This design is easily compile with the existing system this design content two rolling part and a reciprocating part which is used to convert circular motion into reciprocating motion and vice versa. The lift is moving up and down that's the mechanical energy converts that's specific system into electrical energy.

Keyword*: *Electrical Energy, Reciprocating, Rolling.

I. INTRODUCTION

An elevator system, elevator providing a self generating power source. The system converts kinetic energy of an elevator cab movement into electrical energy used to regulate the speed of descent. The elevator system can be structured in numerous ways and includes either a generator or a motor in generator mode, driven by a system to the elevator cab. The present invention relates to a self-powered for elevator systems. More particularly, the

present invention pertains to the use of the kinetic energy of an elevator cab movement to generate electrical energy to regulate the speed level.

II. BACKGROUND OF THE INVENTION

Elevator systems and controls for such systems are known in the art. Such systems and controls use a wide variety of designs to achieve numerous objectives, and the basic principle of balancing an elevator cab against assembly driven by a motor. For years, building designers and code authorities have recognized the necessity of emergency power in buildings to ensure that elevator cabs. Moreover, most elevator systems currently require building power distribution systems to provide transfer switches and emergency feeders for elevators and main distribution emergency switchboards and emergency generators sufficiently large to cover elevator loads, all of which result in additional costs and inefficiencies. Thus, it would be advantageous to have an elevator system that during a power outage or any other occasion when needed accomplishes the controlled descent of the elevator cab without a battery or fossil fuel based generator to drive the elevator motor, but rather accomplishes the initial descent of the elevator cab due to gravitational forces and the heaviness of the elevator cab relative to an attached counterweight, and which then converts kinetic energy of the movement elevator cab into electrical energy used to control the speed of descent of the elevator cab.

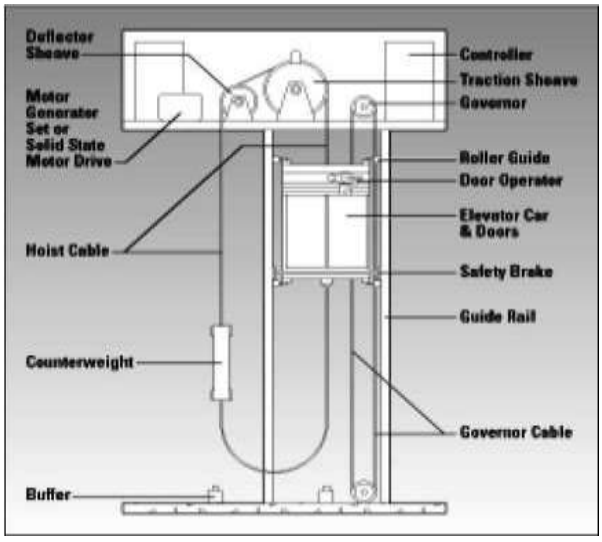

Figure 1: Basic Diagram of Building Lift

III. PROPOSED SYSTEM

The invention and the preferred modes of use will best be understood by reference to the following detailed description of an illustrative embodiment. A control block diagram of a self generating elevator emergency power source for an elevator system using a reciprocating and an electrical generator. A control block diagram of self generating elevator emergency power source for an elevator system using a reciprocating and an elevator motor in generator mode.

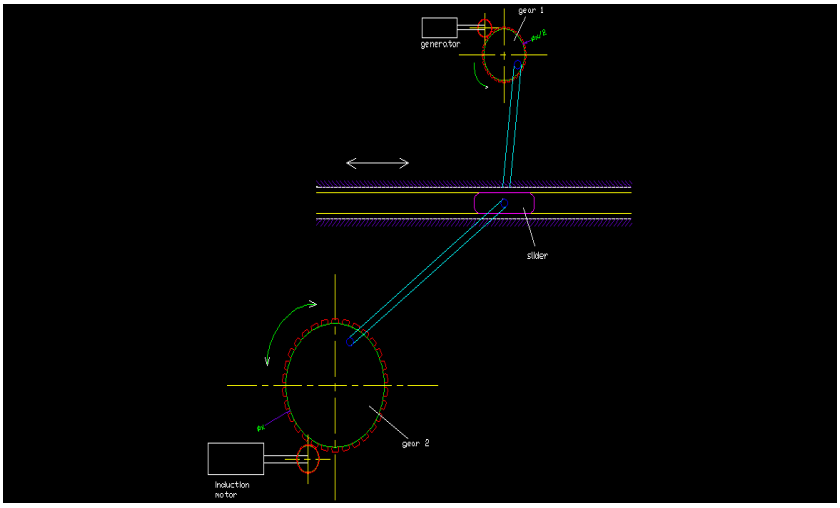

Figure 2: Proposed Mechanism

IV. DETAILED DESCRIPTION

The present invention is based on utilizing the kinetic energy of an elevator cab movement due Reciprocating action of the elevator cab. The movement elevator cab attached to a mechanical system of shafts and pulleys drives either a separate generator or an elevator motor operating in generating mode, converting the kinetic energy of the movement elevator cab into electrical energy. The torque generated by a separate generator or elevator motor in generating mode is directed against torque produced by movement elevator cab and when controlled, a controllable speed of descent to a preset or selected floor can be achieved which provides braking power for a controlled speed of descent to a preset or selected floor, comprising: an a building distribution system electrical supply panel, an elevator controller with an integral battery to support control during power loss or interruption, an electrical drive motor, a load bank, a thiristor or transistor switch or similar operative device, a summing device to sum all control signals and to generate a resultant control signal, a tachogenerator speed feedback device, a dedicated emergency descent controller with pulse width modulation (PWM) output, a mechanical system of shafts and pulleys and respectively, an elevator cab, an alternating or direct current electrical generator, a cable, a permanent counterweight, a detachable counterweight, electrically held spring release locks, detachable counterweight free fall catchers, elevator brakes, a counterweight rail system, and an elevator cab rail system.

The elevator controller with an integral battery to support control during power loss receives power from a building distribution system via the electrical power supply panel. The elevator controller drives the elevator drive motor. The elevator drive motor is connected to the elevator cab via the mechanical system of shafts, pulleys and drives the elevator cab up and down guided by the elevator cab rail system. The elevator controller also is connected to electrically held spring release locks. The bottom part of the spring release locks is coupled to the detachable counterweight, and the top part of the spring release locks is coupled to the permanent counterweight, such that when the permanent counterweight and detachable counterweight come together the locking mechanisms of the spring release locks on each of the two counterweights and engage and thereby join the permanent counterweight and detachable counterweight together to act as a single counterweight. Both the

permanent counterweight and the detachable counterweight are guided by a counterweight rail system. Free fall catchers are coupled to the detachable counterweight. When the spring release locks are engaged during normal operation, the spring release locks lock the permanent counterweight to the detachable counterweight, comprising the total weight offsetting the weight of the elevator cab through the connecting cable and counterweight pulley system.

When the elevator controller senses a power loss in the electrical supply panel, the elevator controller cuts off control voltage to the electrically held spring release locks, causing the spring release locks to disengage the detachable counterweight from the permanent counterweight upon detachment, the detachable counterweight descends under its own weight until the speed of the detachable counterweight exceeds a preset value, at which point the free fall catchers stop the descent of the detachable counterweight by clamping onto the counterweight rail system. The elevator controller is also connected to the elevator brakes, and when the elevator controller senses a power loss in the electrical supply panel, the elevator controller causes the elevator brakes to be released and held in a released position.

Due to the heavier weight of the elevator cab relative to the permanent counterweight, and due to the elevator brakes being held in the released position, the elevator cab begins movement under its own weight after detachment of the detachable counterweight. The movement elevator cab is connected to the alternating or direct current electrical generator through the cable, and mechanical system of shafts and pulleys and respectively, and the descent of the elevator cab thereby causes the cable to rotate the counterweight pulley, thereby through the mechanical system of shafts and pulleys driving the electrical generator. The alternating or direct current generator is connected to the load bank via the thiristor or transistor switch or similar operative device. The dedicated emergency descent controller with pulsewidth modulation (PWM) output is connected to the thiristor or transistor switch or similar operative device, and thereby regulates the generator current through the load bank.

The elevator controller directs the elevator drive motor to rotate the counterweight pulley to raise the elevator cab and correspondingly cause the attached permanent counterweight to descend until the top half of the release locks coupled to the bottom of the permanent counterweight engages the top half of the release locks coupled to the top of the detachable counterweight, at which point the release locks engage and thereby couple the permanent counterweight to the detachable counterweight, restoring the elevator system to normal operation.

In an alternative embodiment, an elevator system, instead of using the electrical generator of to generate electrical energy during power loss or interruption, the system uses the elevator drive motor with a motor mode operation switching contactor. The elevator controller is connected to the motor mode operation switching contactor.

In an alternative embodiment, an elevator system, instead of using the electrical generate electrical energy during power loss or interruption, uses the elevator drive motor with a motor mode operation switching contactor. Further, rather than using the detachable counterweight with release locks and free fall catchers, the system uses the permanent counterweight that is lighter than the elevator cab so that when the elevator controller after sensing power loss directs that the elevator brakes release and be held in a released position, the elevator cab begins movement due to its heaviness relative to the permanent counterweight.

In another embodiment of the invention, a retrofit kit can be installed in existing elevator systems to accomplish an elevator system. The retrofit kit is comprised of a replacement counterweight consisting of a permanent counterweight joined to a detachable counterweight with free fall catchers through electrically held spring release locks or other like devices. The top half of the spring release locks is coupled to the bottom of the permanent counterweight, and the bottom half of the spring release locks is coupled to the top of the detachable counterweight. The retrofit kit includes a small battery for the elevator controller to support control during power loss, which battery is integral to the elevator controller. The retrofit kit further includes an alternating or direct current electrical generator, the output of which is connected to the load bank via the thiristor or transistor switch or similar operative device. The retrofit kit includes a dedicated emergency descent controller with pulsewidth modulation (PWM) output connected to the thiristor or transistor switch or similar operative device, which thereby regulates the generator current through the load bank.

In an alternative embodiment, a retrofit kit can be installed in existing elevator systems to accomplish an elevator system. A difference between the elevator retrofit kit based and the elevator retrofit kit based is that instead of being comprised of the electrical generator to generate electrical energy during power loss or interruption, the retrofit kit is comprised of the elevator drive motor with the motor mode operation switching contactor. When installed, the retrofit kit functions in a manner consistent with the elevator system described.

In yet another embodiment, a counterweight device is comprised of the permanent counterweight and the detachable counterweight with free fall catchers, the permanent counterweight and detachable counterweights being coupled together by electrically held spring release locks or other like devices when the locks are engaged. The bottom part of the spring release locks is coupled to the detachable counterweight, and the top part of which spring release locks is coupled to a permanent counterweight.

When the permanent counterweight and detachable counterweight come together, the locking mechanisms of the spring release locks on each of the two counterweights engage and thereby join the permanent counterweight and detachable counterweight together to act as a single counterweight. Both the permanent counterweight and the detachable counterweight are guided by the counterweight rail system. Free fall catchers are coupled to the detachable counterweight. A power loss to the electrically held spring release locks, whether by direction of an elevator controller or otherwise, causes the spring release locks to disengage. Upon detachment, the detachable counterweight descends under its own weight until the speed of the detachable counterweight exceeds a preset value, at which point the free fall catchers stop the descent of the detachable counterweight by clamping onto the counterweight rail system. After return of normal power and upon the permanent counterweight being lowered to the detachable counterweight, or upon the detachable counterweight being raised to the permanent counterweight, the electrically held spring release locks engages and thereby couples the permanent counterweight to the detachable counterweight.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments that fall within the true scope of the invention. In the existing system the new

design is used for converting unutilized mechanical energy into electrical energy and it is compactly fitted into headroom. This new design is specific to the regenerate the electrical energy from mechanical energy of the lift which is stored in battery and it will use whenever the light is off This design is easily compile with the existing system this design content two rolling part and a reciprocating part which is used to convert circular motion into reciprocating motion and vice versa. The lift is moving up and down that's the mechanical energy converts that's specific system into electrical energy.

V. CONCULSION

Various modifications of the disclosed embodiments as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments that fall within the true scope of the invention.

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TESTING THE IMPACT OF INFLATION AND REPO RATE ON THE GOLD PRICE: EVIDENCE FROM INDIA

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ABSTRACT

This paper is an attempt to test the dynamic relationship and study the impact of Repo rate, and persisting inflation rate on the Gold price. The study used Regression Model to determine significant relationship between dependent and independent variables. The empirical results have found there is significant negative relationship between the Gold price and Repo rate that is increase in Repo rate resulted decrease in the Gold price. Another interesting finding of the study is the Gold prices and inflation rate is also dependent and positively correlated this means increase inflation leads to increase in the Gold price. The results of the study are valuable for both academicians and investors. The investors take account of these macro economic factors before investing in the Gold to increase portfolio's risk free adjusted rate of return. Gold is a good diversifier too of the portfolio.

Key Words: Diversification, Gold Price, Inflation Rate, Investment, Investors, Macroeconomic Factors, Rate of Return, Repo Rate

I INTRODUCTION

Diversified Portfolios which include assets such as private equity, hedge funds, real estate, debt funds and commodities can be enhanced by adding a discrete allocation to gold as a foundation. Diversification strives to smooth out unsystematic risk events in a portfolio so that the positive performance of some investments will neutralize the negative performance of others. Investors are always looking to amplify their risk-adjusted returns and add diversification. The gold is not only an ideal source of diversification for an investor's portfolio, but also provides a foundation which investors rely on to manage risk and preserve capital more proficiently, especially in times of financial chaos when stability is most needed [13]. It has acted as a multifaceted metal down through the centuries, having similar attributes to money in that it acts as a store of wealth, medium of exchange and a unit value. Gold has also played an important role as a precious metal with significant portfolio diversification properties. Investors of all types have increasing proportion of gold in their portfolio allocation as leading to a more

balance portfolio. The changes in the interest rate, the covariance of returns to gold with a diversified portfolio of other assets, default risk, the convenience yield and particularly the gold lease rate can seriously disturb the equilibrium and generates considerable short-run volatility [1]. The study on a gold pricing model has concluded that gold price has a significant positive relationship with unexpected inflation [14]. The stock price index and long-term interest rates are negatively correlated as per the empirical study [15]. The research work published by World Gold Council primarily focuses on the mythological and cultural significance of gold in India. The study found that Indians love gold and this has been explained logically and culturally [16]. Logically, gold is a tangible investment, unlike shares and bonds; a portable investment like property and a beautiful ornament, one that can be worn daily on the body as jewellery. But the same can be said of diamonds and other precious metals. The value of gold stems from jewellery to a most important avenue of wealth accumulation by the low and middle-income households in rural and urban areas. The key drivers for the gold demand were real income level of the population, expectation of higher gold price, exchange rates, as an alternative instrument of saving, gold as an equity security, controlled supply conditions, the correlation between savings and uncertainty. Empirical studies reveal that gold demand is not only price sensitive but also affected by macroeconomic indicators and financial variables [17]. The relationship was examined over the periods, with meticulous attention paid to the hedging properties of gold in episodes of economic or political havoc. There are a number of distinctive qualities that separate gold from the rest of the commodities, such as the U.S. dollar is weakening, Inflation fears, Emergence of China and India, Supply constraints, Geopolitical instability. But gold is viewed as a safe haven during times of political or economic crisis.

II REVIEW OF LITERATURE

There are many studies conducted on the pricing mechanism of gold in the past. Although various different variables are examined in these studies but some variables have or have not significant impact on gold price mechanism. The significant variables such as growth, inflation, global money supply and the US dollar exchange rate, which affects the demand of the gold outside the Euro zone [18]. The crude oil price and inflation have important role in the gold market [2]. There is a positive correlation between gold prices and crude oil prices. A negative and significant relationship is found between the returns of gold and US Dollar [19]. There is inverse relationship between Gold price and Dollar value, positive correlation between Gold price and Crude oil price, Gold prices and repo rates are negatively correlated [3]. The gold prices and the U.S. dollar exchange rate are considerably related to each other [4]. By applying newly developed econometrics methods, found that gold is a safe asset against fluctuations in the USD. The inclusion of gold in a portfolio leads to a risk reduction because the correlation between the gold and stocks was close to zero [5]. The gold does not depend on the business cycles as compare to other commodities, which makes gold a good portfolio diversifier [6]. The study finds high sensitivity of gold to real interest rates, its role as safe-haven and store of value leads to a counter-cyclical reaction to astonish news, in comparison to other financial commodities [7]. Gold also shows high sensitivity to negative surprises that may lead investors to become risk averse. The bond market plays its role as a hedge for the equity market [20]. The gold consistently acts as safe haven when exchange rates plunge considerably in the US and the UK markets, which confirms gold as a monetary

asset [8]. The investors might be able to predict the gold futures by the dollar index and inflation index [21]. The investors can predict the inflation index by the oil price and then deduct the fluctuation in gold futures. The volatility of oil and gold are mean reverting this means there exist a strong anti-correlation between oil and gold volatility [9]. The inclusion of oil and gold in the portfolio construction maximize the investors risk free adjusted rate of return. The exchange rates have a direct influence on gold prices, oil prices and stock market index [10]. The fluctuations in gold prices are driven by gold itself rather than oil and other indices. Gold plays a significant role with leading variation in exchange rates [22]. The interest rates, gold price and oil price are negatively correlated with dollar. So there is causal correlation among them [11]. The gold investment is safe for the investors and could be categorized as safe haven [12].

III OBJECTIVES

- To study and analyze the impact of inflation rate on the Gold prices.
- To study and analyze the impact of repo rate on the Gold prices.

IV RESEARCH METHODOLOGY

For causal research to establish the quantitative relationship between prices of gold and other factors (daily prices of gold and other factors) were collected from the various secondary sources like newspapers, internet, magazines, books, journals were referred to understand the relationship between price movements of gold and other factors. The major data sources are **WGC** (World Gold Council), Reserve Bank of India, and Ministry of commerce and industry. In addition to usage of statistical packages the quantitative data was analyzed through regression analysis and trend analysis technique. For this study, the period of six years and six months is taken commencing from April 2009 to December 2014 is considered. During which daily prices of gold and other selected factors were taken into account and then converted into average monthly prices.

4.1 Hypotheses

1. H_0: The Repo rate does not affect the gold prices.

2. H_0: The Inflation rate doesn't affect the gold prices.

4.2 Tools and techniques

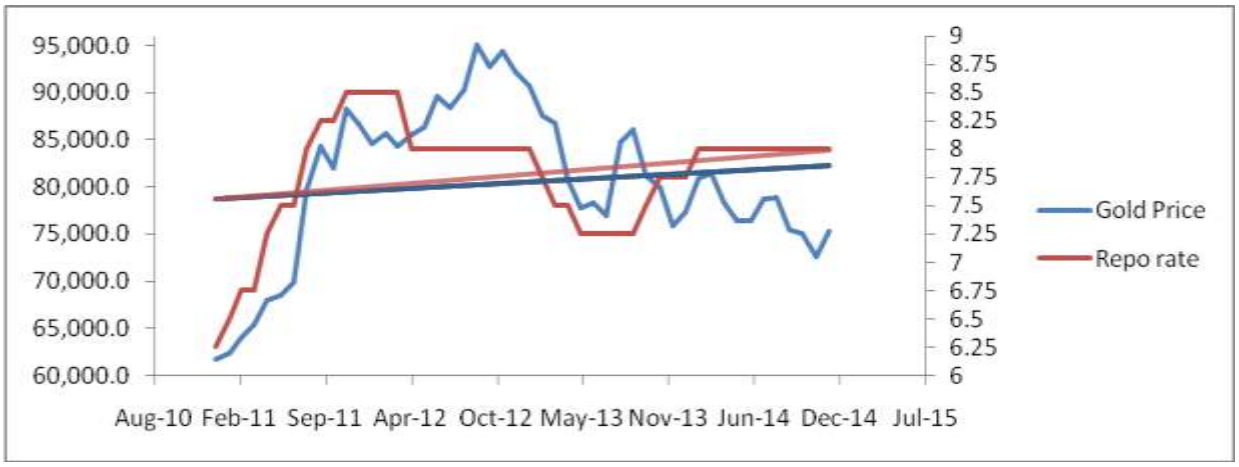
A comparative analysis of various factors has been done on the various parameters such as Standard Deviation, Regression, and correlation to make possible the tedious task of analysis of these factors. Further analyzing the factors will suggest the investors that whether it will be profitable for the investors to invest in gold or not.

4.3 Gold Price Vs Repo Rate

Repo Rate is that rate at which the commercial banks borrow money from the **RBI (**Reserve Bank of India). It is an excellent measure to curb persisting inflation rate. This ultimately reduces the money supply in the economy and thus helps in arresting inflation. When the repo rate will be high, the borrowing from the banks will be low which will actually reduce the purchasing power of the public. This will reduce the investment in gold and it will ultimately reduce the price the gold.

H_0 - The Repo rate does not affect the gold prices.

Graph1: Trend Analysis of Repo Rate and Gold price:



Analysis Overview

Regression Statistics

Multiple R	0.654
R Square	0.428
Adj R Square	0.415
Standard Error	6360.544
Observations	48

ANOVA

	df	*SS*	*MS*	*F*	*Sign. F*
Regression	1	1.39E+09	1.39E+09	34.44656	1.40E-05
Residual	46	1.86E+09	40456520		
Total	47	3.25E+09			

	Coeffs	*St Error*	*t Stat*	*P-value*	*Lower 95%*	*Upper 95%*
Intercept	-2350.39	14143.97	-0.166	0.868	-30820.7	26119.95
Repo rate	-1065.93	1815.081	5.869	0.000	6999.358	14306.49

Tabulated t value = 2.764

Significant correlation with r = 0.654. Approximately 42% of variation in gold prices is explained with change in repo rate and the rest due to some other variables. Significant linear regression with p value = 0.00.

Regression equation y = -1065.93x - 2350.39

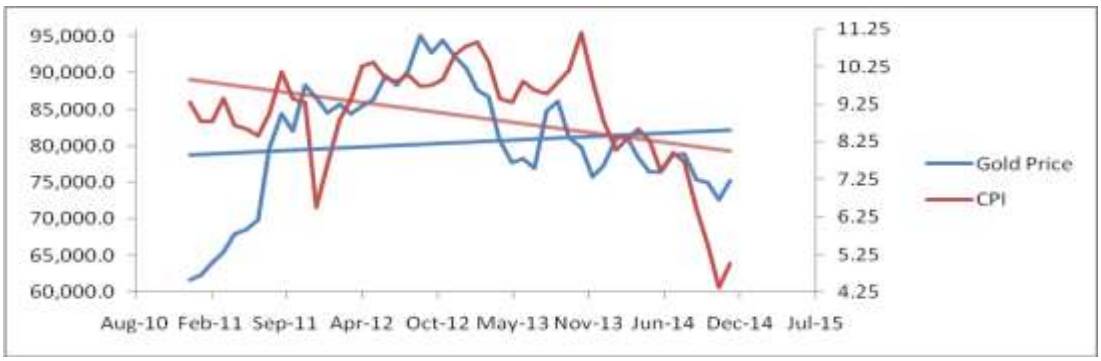
From the R value = 0.654 it can be seen that there is significant correlation between the repo rates and the gold prices. Because the R value is above 0.5 which prove that there is significant correlation. Also the observed t value is 5.869 greater than tabulated t value which is 2.764. This shows that null hypothesis is rejected and alternative hypothesis accepted that repo rates given by the RBI do affect the gold prices. There is negative correlation exists between repo rate and gold prices.

4.4 Gold price VS Inflation rate

Gold has always been considered a good hedge against inflation. Rising inflation rates typically appreciates the gold prices. Traditional theory implies that the relative price of consumer goods and of such real assets as land and gold should not be permanently affected by the inflation. A change in the general rate of inflation should, in equilibrium, cause an equal change in the rate of inflation for each asset price. While calculating the price of gold there are two inflation rates. One is Gold internal inflation rate, which is change in its production from its mines and other is monetary inflation rate. The price of gold over the medium to long term is determined by its inflation rate relative to that of the currency you want to measure it with. The most fiat currency inflation rates, running substantially higher than gold's inflation rate it is easy to see why the gold price will continue to increase over time, and why it has consistently increased over time.

H_0: The Inflation rate doesn't affect the gold prices.

Graph 2: Trend analysis of Inflation rates and Gold Prices



Analysis Overview

Regression Statistics		
Multiple R	0.795	
R Square	0.556	
Adj R Square	0.338	
St Error	772.797	
Observations	48	

ANOVA

	df	*SS*	*MS*	*F*	*Sign. F*
Regression	1	5.089E+08	5.089E+08	8.527E+00	5.404E-03
Residual	46	2.746E+09	5.969E+07		
Total	47	3.255E+09			

	Coeffs	*St Error*	*t Stat*	*P-value*	*Lower 95%*	*Upper 95%*
Intercept	6044.42	6936.930	8.721	0.000	46531.113	74457.743
Inflation	2232.19	764.434	2.920	0.005	693.463	3770.917

Tabulated t value = 3.8543

Significant correlation with r = 0.795. Approximately 55% of variation in gold prices is explained with change in inflation rate and the rest due to some other variables. Significant linear regression with p value = 0.005.

Regression equation y = 2232.19- 6044.42

Also from the t-value it can be said that the hypothesis assumed can be rejected. The observed t-value is 8.721 which are greater than tabulated value 3.8543. It verifies whatever the studies are until now that is the gold is an inflation hedge. The analysis also shows that inflation rate is positively related with the Gold prices. In addition, it should be noted that increase in inflation rate accounts for increase in investment in gold, as it is an inflation hedge.

V FINDINGS AND CONCLUSIONS

H_0: The Repo rate does not affect the gold prices.

The observed t value is 5.869 which greater than the tabulated t value is 2.764 and imply the acceptance of alternate hypothesis, i.e. the repo rate have a significant impact on gold prices. There is positive correlation exists between the repo rate and the gold price.

H_0: The Inflation rate doesn't affect the gold prices.

The Inflation rate doesn't affect the gold prices. By observing the t-value it is concluded that the hypothesis assumed is rejected i.e. alternate hypothesis is accepted (observed T-value is 8.721 which is greater than tabulated t-value 3.854) and therefore Gold prices do depend upon inflation rates.

In India, gold is one of the foundation assets for Indian households in the form of investment. It is viewed as secure, liquid investment. Two factors have been considered here which influence the gold prices and the analysis of these factors reveals that: Gold prices and repo rates are negatively correlated. It can be explained as the repo rate increases the gold prices decreases. Because increase in repo rate reduces the flow of money in the economy and purchasing power of individuals decreases. The inflation rate and gold prices are positively correlated with each other. When there is increasing trend of inflation in the economy the gold prices increase too. This satisfies the gold is inflation hedge in times of high inflation trend.

From the study it is concluded that the selected factors such as repo rate and inflation rate announced by RBI (Reserve Bank of India) do have impact on the gold price. Investors should take account of these factors before to invest in the gold to maximize his risk adjusted rate of return.

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FAULT TOLERANT CONTROL FOR SERIES COMPENSATORS FOR POWER SYSTEM STABILITY IMPROVEMENT

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ABSTRACT

This paper presents a fault –tolerant indirect adaptive neuro-controller (FTNC) for controlling a Series Compensator, which is connected to a power network. The FTNC consists of a sensor evaluation and restoration scheme (SERS), a radial basis function neuro-identifier (RBFNI) and a radial basis function neuro-controller (RBFNC). The SERS is designed using the auto-associative neural networks(auto-encoder). This FTNC is able to provide efficient control to the Series Compensator when single or multiple crucial sensor measurements are unavailable. The validity of the proposed model is examined by simulations inMATLAB/SIMULINK environment.

Keywords: CSC, TCSC, Fault –Tolerant Control, Neural Networks, Series Compensator.

1.INTRODUCTION

Power utilities of today use a variety of technologies to reduce the impact of disturbances in the power grid, lowering the risk of blackouts. Many of these are commonly referred to as Flexible AC Transmission Systems(FACTS) devices. Two well known FACTS devices are the Thyristor Controlled Series Compensator(TCSC) and the Thyristor Switched Series Compensator(TSSC) belonging to the group of Controlled Series Compensators(CSC). CSC are based on the principle of varying of the power line series reactance in order to control power flows and enhance system stability. The most important phenomena which threaten the stability of power systems are poorly damped low frequency electromechanical oscillations, first-swing instabilities and voltage instabilities.

In terms of the control objectives, various control schemes, based on the conventional linear PI controllers, have been designed for the internal control of the Series Compensator [3]-[6]. From proposed references , the neuro-controller was shown improved transient performance over the conventional linear PI controllers(CONVC).

However, control of nonlinear plants in power systems relies on the availability and the quality of sensor measurements. Measurements can be corrupted or interrupted due to sensor failure, broken or bad connections, bad communication, or malfunction of some hardware or software (these are referred as missing sensor measurements in this paper). If some sensors fail to provide the correct information, the controllers cannot guarantee the correct control behavior, for the plant based on the faulty input data. Therefore, fault-tolerant measurements are an essential requirement for system control. For many systems, certain degrees of redundancy are present among the data collected from various sensors.If the degree of redundancy is sufficiently high, the readings from one or more missing sensors may be able to be accurately restored from those remaining healthy sensor readings. Conventional methods in recovering missing sensor data are based on the analysis of the system model, e.g., the state estimation methods. The drawbacks of these methods have been discussed in [7],[8].

This paper proposes a fault-tolerant indirect adaptive neuro-controller(FTNC) for the internal control of a Series compensator connected to a power network. This FTNC contains a SERS cascaded with a radial basis function neuro-identifier(RBFNI) and a radial basis function neuro-controller(RBFNC),as shown in Fig.1. The RBFNI is trained to provide a dynamic predictive plant model at all times; this plant model is then used for training the RBFNC; the RBFNC in turn generates the control signals to drive the outputs of the actual plant to the desired values[6]. The SERS is used to evaluate the integrity of the crucial sensor measurements that determine the behaviors of the RBFNI and the RBFNC. If one or more sensors are missing, the SERS searches in its input space for the optimal estimates of the missing data.The restored values of the missing data from the SERS, together with the remaining data read directly from the healthy sensors, provide a set of complete inputs to the RBFNI and the RBFNC. This guarantees a fault-tolerant control for the Series compensator.Simulation studies are carried out with single and multiple time varying current sensors missing in order to evaluate the performance of the proposed FTNC scheme.

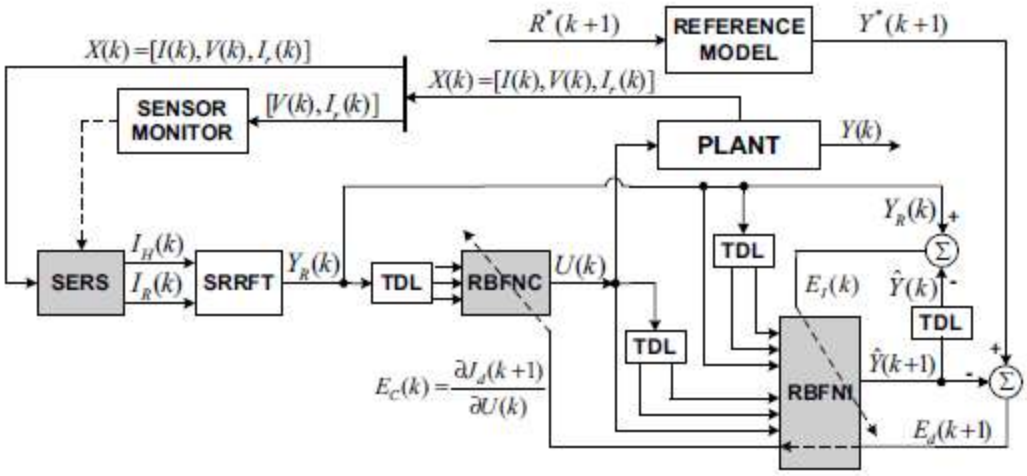

Fig.1.Schematic diagram of the fault-tolerant indirect adaptive neuro-controller(FTNC) connected to the plant:$R^*=[Q^*,P^*]$, $Y^*=[i_q{}^*,i_d{}^*]$, $U=[v_{eq}, v_{cd}]$, $Y= [i_q,i_d]$, $Y_R= [i_{qR}, i_{dR}]$, $Y=[i_q{}^*,i_d{}^*]$, $I=[i_a, i_b, i_c]$ $V=[v_{ca},v_{cb},v_{cc}]$, and $Ir=[i_{ra},i_{rb},i_{rc}]$. SRRFT means synchronously rotating reference frame transformation.

II REDUCED GRID MODEL

In order to design a damping controller for inter-area power oscillations, a system model is required. The nature of inter-area oscillations is often such that there is a dominant mode of oscillation which may be poorly damped. With this in mind, a simple way to reduce the total power grid is to approximate the grid as a system of the form seen in Fig.2. The reduced model of the power system using a Center Of Inertia (COI) reference frame consists of two synchronous machines with interconnecting transmission lines. In this work , the model parameters are updated continuously by the controller using the locally measured responses in the CSC line active power(P_{line}) to changes in the variable series reactance.

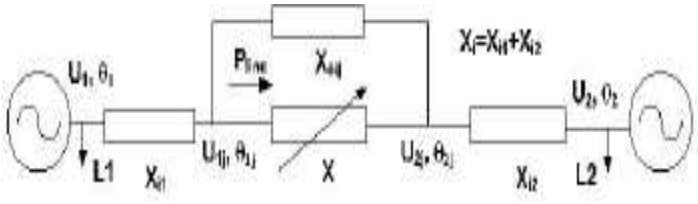

Fig.2 The reduced grid model used by the controller

The line where the CSC is installed is represented by a variable, known reactance X. The model is characterized by four additional parameters: one series reactance X_{i1} ,one parallel reactance X_{eq}, the dominant angular frequency of the power oscillation ω and the damping exponent of this oscillation mode –σ. The machine terminal voltage phasors characterized by the magnitudes $U_{1,2}$ and the phase angles $\Theta_{1,2}$ are assumed to be well controlled and thus constant in magnitude. When applied to real power systems, the model [1] may represent two different grid areas with lumped moments of inertia and their interconnecting power lines. The load in each of these areas is modeled as constant voltage-independent loads.

III THEORY

3.1. Estimation of the reduced model parameters

Since an adaptive control appoach is used, the parameters of the grid where the FACTS device is placed are estimated continuously by the controller according to the model of Fig.2. The controller is time-discrete in nature making it possible for the estimation routines to be developed based on the step response of the reduced system in Fig.2 to changes in the CSC reactance. In [1], equations governing the step response in active power on the

reactance controlled line when a step in the line reactance is applied to a system at rest were derived. It is also possible to derive relations for the step responseof the system when it is initially subject to an electro-mechanical oscillation. Such relations are used by the controller proposed here to estimate the grid parameters in real-time.

3.2 Estimation of the CSC line power frequency content

In order to use the estimation techniques outlined above and to determine the input and timing for the damping controller it is necessary to separate the average and oscillative components of the line active power in real-time.This is done using a Recursive Least Squares(RLS) algorithm[9].In this paper , the algorithm is used based on the assumptionthat the line power is composed of a zero frequency component(the average value) and a component which has a known frequency range(the power oscillation frequency). The algorithm utilizes an expected oscillation frequency when no oscillations are at hand. At any event that causes power oscillations, the frequency parameter is adapted to the actual oscillation frequency by a PI-controller. The algorithm gives a real-time estimation of the line average power (P_{av}), oscillation amplitude (P_{osc}), frequency (ω) and phase (φ_{osc}).

3.3. Power oscillation damping

The controller developed here is based on a time-discrete approach to power oscillation damping. The approach is somewhat similar to that of [6]. In [2] it was shown that a power oscillation in a power system characterized by one dominant mode of oscillation can be damped by changing a selected line series reactance in one step of a certain magnitude at a carefully selected time instant. The necessary reactance magnitude can be determined knowing the system parameters according to the model of Fig.2. It was also shown that a more realistic controller can be built on the principle of (ideally) eliminating the power oscillation in two discrete reactance steps separated in time. This objective can also be met simultaneously as the active power flow on the reactance controlled line is changed to a pre-defined new set-point as shown in [3]. The time instants of the steps must be chosen such that they coincide with peaks(positive and negative) in the power oscillation. This gives a controller with a time-discretization determined by the oscillation frequency.

IV MULTI-OBJECTIVE CONTROLLER

Now, a controller for power oscillation damping (POD), first-swing stability improvement (FSW) and active power flow control can be designed. The first-swing controller has the highest priority and inhibits the other controller parts if initiated. Generally, a fault in the system first leads to a risk of transient instability which initiates the first-swing controller. When the first-swing controller has performed its sequence there is commonly a power oscillation in the system which is detected by the RLS algorithm. This oscillation triggers the damping controller which has a built –in power flow control feature for fast control of the power on the line after a fault. Since the damping controller/fast power flow controller is only active when power oscillations are present, a seperate slow PI-controller

is necessary for long-term power flow control. These controllers contribute the terms X_{POD} , X_{PSW} and X_{PI} to the reactance of the CSC-X_{TCSC} (Fig.3). All controllers use the CSC line active power (P_{line}) or estimations of it as input signals. The first swing controller also uses the CSC line current (I_{line}) as an input signal.

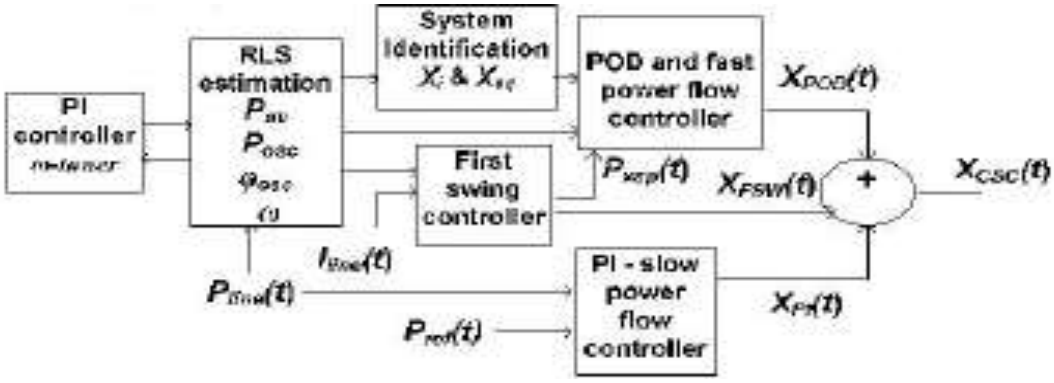

Fig.3: Principal schematic of the CSC controller

V FAULT-TOLERANT INDIRECT ADAPTIVE NEURO-CONTROLLER

5.1. Design of RBFNI and RBFNC

The RBFNI The RBFNI and RBFNC are each a three-layer RBF network with the Gaussian density function as the activation functions in the hidden layer. The overall input-output mapping for the RBF network, $f : X \in R^n \rightarrow Y \in R^m$ is

$$\hat{y}_i = b_i + \sum_{j=1}^{h} v_{ji} \exp\left(-\frac{\|x - C_j\|^2}{\beta_j^2} \right) \qquad (1)$$

where x is the input vector, $C_j \in R^n$ is the center of the j^{th} RBF units in the hidden layer, h is the number of RBF units, b_i and v_{ji} are the bias term and the weight between hidden and output layers respectively, and y_i is the i^{th} output. The RBFNI is used to provide a dynamic predictive plant model at all times. This model is then used for training the RBFNC. The RBFNC is used to replace two conventional PI controllers (PId and PIq) in Fig. 3. The inputs of the RBFNC are the plant outputs at time k-1, k-2 and k-3. It in turn generates the control signals as the plant inputs in order to drive the plant outputs to the desired values. The detailed design and training process for the RBFNI and RBFNC has been discussed in [6].

5.2. Missing Sensor Restoration Algorithm (MSR)

Figure 4 shows the structure of a MSR block [7], [8]. It consists of a dynamic auto-associative neural network (autoencoder).

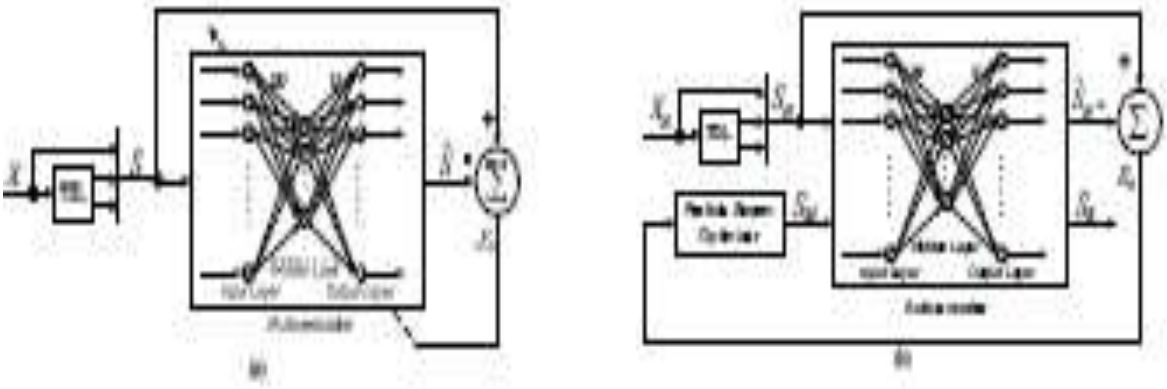

Fig.4 Overall structureof MSR a) Training phase of the auto-encoder.b) On-line restoration of missing sensor data.

1) Auto-Encoder (Fig. 4(a)): The auto-encoder is a multilayer perceptron (MLP) neural network with butterfly

structure [7], [8]. It has the same number of inputs and outputs, but the number of neurons in the hidden layer is less than that of the inputs. This particular structure creates a bottleneck in the feedforward path of the auto-encoder, enabling it to capture the correlations between the redundant inputs. The inputs of the auto-encoder, *S*, consist of the vector, *X*, at the present time step as well as at the previous two time steps (*i.e.*, $S(k) = [X(k), X(k\text{-}1), X(k\text{-}2)]$). The use of the timedelayed inputs enables the auto-encoder to capture the auto-correlations of each variable in its input vector *X*. The auto-encoder is firstly trained without any missing sensor. During the training, the two PI controllers (PId, PIq) are deactivated as shown in Fig. 3 and the steady state plant inputs v_{cqS} and v_{cdS} are disturbed by pseudorandom binary signals (PRBS) from an external source at each time step *k*, given by

$$PRBS\_\, v_{cd}(k) = 0.1 \,|\, v_{cdS} \,|\, [rand2(k) + rand3(k) + rand5(k)]/\, 3 \qquad (2)$$

$$PRBS\_\, v_{cq}(k) = 0.1 \,|\, v_{cqS} \,|\, [rand2(k) + rand3(k) + rand5(k)]/\, 3 \qquad (3)$$

where *rand*2, *rand*3 and *rand*5 are uniformly distributed random numbers in [-1, 1] with frequencies 2 Hz, 3 Hz and 5 Hz, respectively; $|v_{cdS|}$ and $|v_{cqS}|$ are the magnitudes of v_{cqS} and v_{cdS} respectively. By feeding forward the data through the autoencoder and adjusting its weight matrices (using backpropagation algorithm), *W* and *V*, the auto-

encoder is trained to map its inputs to its outputs. The detailed description of the auto-encoder training process has been given in [9].

VI SIMULATION RESULTS

The dynamic performance of the proposed FTNC is evaluated at two different operating points by applying three phase short circuit and missing sensor tests.

6.1. Tests at the Operating Point Where Controllers are Designed

The RBFNC is trained and the CONVC is tuned at a specific operating condition (called OP-I), where the generator operates with a pre-fault rotor angle of 42.6°. A three-phase short circuit is applied to the receiving end of line 2 at *t* = 15 s and 100 ms thereafter, line 2 is cleared out from the system. Three missing sensor tests are then applied from *t* = 15.1 s during this post-fault transient state: 1) Case I – *ib* missing; 2) Case II – *ib* and *ic* missing; 3) Case III – *ia*, *ib* and *ic* missing.

Figures 5,6 and7 show the results of the rotor angle δ for Cases I, II and III, respectively. These results show that the damping control of the FTNC is more efficient than that of the CONVC during the post-fault transient state. During the first swing after the fault is applied, the FTNC is already providing significant damping compared to that provided by the CONVC. By continuously training the RBFNI and the RBFNC, the FTNC drives the plant successfully and quickly to a new operating point with a rotor angle δ = 46.3° at the steady state. Moreover, comparing the curves by FTNC with and without missing sensors, the transient performance of the FTNC only degrades slightly due to missing sensor data. However, comparing the curves CONVC and the curves FTNC withmissing sensor or sensors, the transient

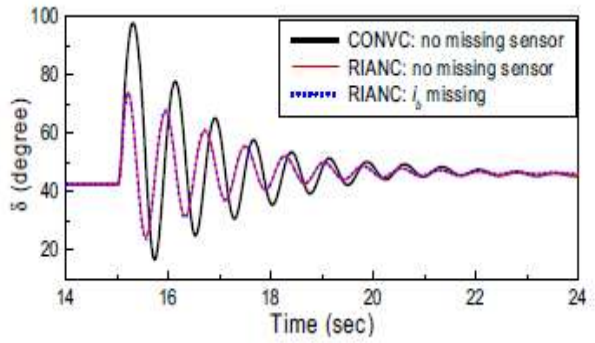

Fig.5. A 100ms three-phase short circuit at 15.0s at OP-I; caseI-ib missing from 15.1s

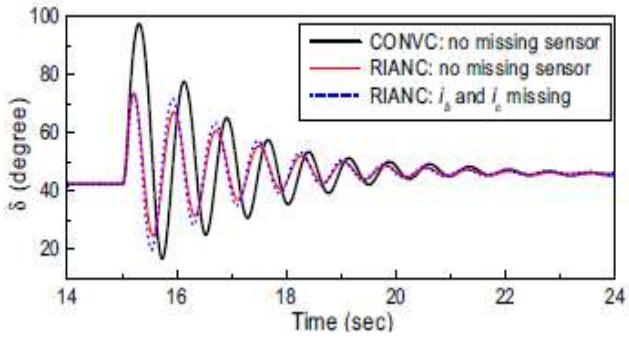

Fig.6. A 100ms three-phase short circuit at 15.0s at OP-I; Case II-ib and ic missing from 15.1s.

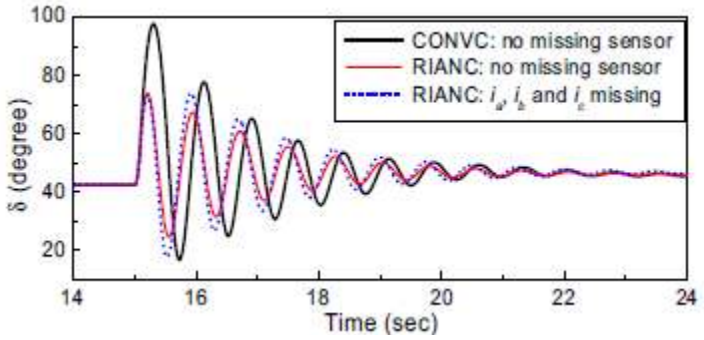

Fig.7 . A 100ms three-phase short circuit at 15.0s at OP-I; case III-ia ib and ic missing from 15.1s.

performances of the FTNC with missing sensor measurements are still better than those of the CONVC used by the TCSC without any missing sensor. In this sense, the proposed FTNC provides a fault tolerant robust control for the TCSC.

6.2. Tests at a Different Operating Point

The transient performance of the FTNC is now re-evaluated at a different operating point (OP-II), where the pre-fault rotor angle of the generator changes to 50.1°; line 1 is now open during this entire test. The parameters of the controllers are the same as those used in the test at OP-I, *i.e.*, the RBFNC has not been trained and the CONVC has not been tuned for OPII; but the SERS has been trained for this operating point. A 100 ms three-phase short circuit is applied to the receiving end of line 2 at t = 15 s. Again, three missing sensor tests same as those in the previous subsection are applied during this postfault transient state.

Figures 8,9and 10 show the results of the rotor angle δ for Cases I, II and III, respectively. These results indicate that the CONVC fails to drive the system back to the steady state after this large disturbance. However, the FTNC still provides the efficient control even if there are sensors missing or not. These results prove that the proposed FTNC provides improved transient performance over the CONVC and a faulttolerant control for the SSSC over a wide range of operating conditions. Under balanced operation, missing one sensor might be simply restored using the relationship $ia + ib + ic = 0$.However, the use of SERS is still necessary because it identifies which sensor is missing. This can not be achievedby only using that relationship. Moreover, power systems might experience unbalanced operations. In this case, the relationship above cannot be used to restore the missing sensor. The use of the SERS to identify and restore the missing sensors under unbalanced operating condition has been discussed and the simulation results have been given in [9].

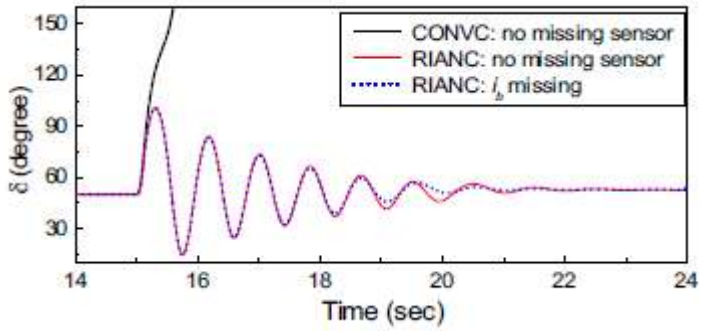

Fig.8 . A 100ms three-phase short circuit at 15.0s at OP-II; CaseI-ib missing from 15.1s.

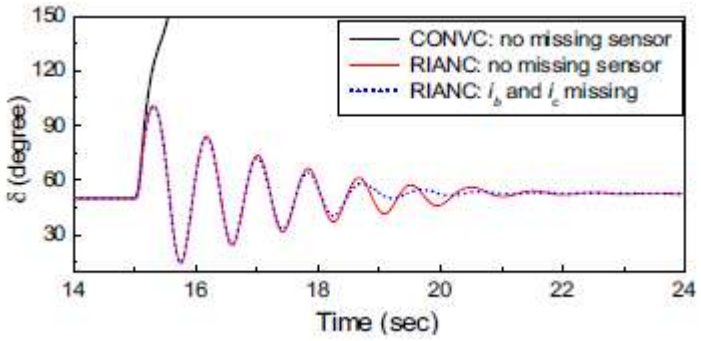

Fig.9. A 100ms three-phase short circuit at 15.0s at OP-II ; Case II-i_b and i_c missing from 15.1s.

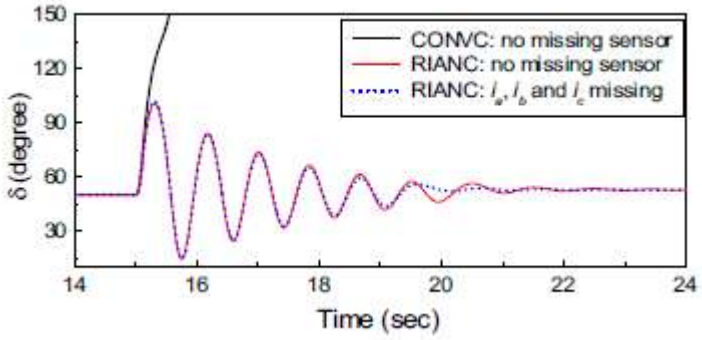

Fig.10. A 100ms three-phase short circuit at 15.0s at OP-II ; Case III – i_a, i_b and i_c missing from 15.1s

VII CONCLUSION

This paper has proposed a fault-tolerant indirect adaptive neuro-controller (FTNC) for the internal control of an TCSC, which combines a suitably designed sensor evaluation and (missing sensor) restoration scheme (SERS), a RBF neuroidentifier (RBFNI) and a RBF neuro-contrroller (RBFNC). The SERS is designed using the auto-

associative neural networks (auto-encoder). This FTNC is able to provide efficient control to the TCSC when some crucial sensor measurements are unavailable. Simulation studies are carried out at two operating conditions for the CONVC and the FTNC without any missing sensor, as well as for the FTNC with single and multiple phase current sensors missing; results show that the transient performances of the proposed FTNC with or without missing sensor measurements are both superior to the conventional linear PI controllers used by the TCSC without any missing sensor over a wide range of system operating conditions.

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OPTIMIZATION OF THE BUCKLING PARAMETERS FOR E-GLASS /EPOXY SANDWICH STRUCTURE USING TAGUCHI APPROACH

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ABSTRACT

The objective of the paper was to investigate influence of buckling test parameters on buckling strength and deformation of e-glass /epoxy sandwich structures using statistical model like Taguchi technique. Three types of epoxy based corrugation i.e. sinusoidal, square and triangle of different core thickness and different strain rate were tested. This research work developed a multiple regression model for correlation between parameters and responses using L9 array. Analysis of variance was used to measure weightage of process parameters. Analysis of the influences of the entire individual input impact parameters on the responses has been carried out and significant contribution of parameters is determined by analysis of variance.

Key Words: ANOVA, Buckling, E-Glass /Epoxy, Process Parameters, Taguchi Technique

I INTRODUCTION

The polymer sandwich structures find many applications such as aerospace, marine, domestic and even sports industries [1] due to their higher stability, high specific strength and easy to repair their structures. But polymer sandwich structures is higher sensitive to buckling [2] due to their lack of poor bonding between reinforcement and polymers due to combination of two heterogeneous structures such as core and laminates face sheet. The buckling behaviour of structure is affected by both materials hence the nature of damage under buckling loads should be investigated carefully for their reliability and safety [3]. Sandwich structures with polymer foam cores could be weak against buckling loads and are therefore subject to several global researches [4].

Buckling loading in complete perforation of the sandwich strucrues are called column buckling, which is caused due to loading speed which will buckled complete sandwich strucures[5]. Many researchers[6] investigated the buckling limit of a variety of o-f sandwich strucrues[7] under five factors such as sandwich density [8], stacking sequence[9], laminate thickness [10], lend / thickness ratio [11] and type of materials. Dear et al. [12] have studied the damage behaviour in honeycomb core sandwich strucrues from the onset of damage to catostropic failure. In same direction many are investigated to find damage behaviour of sandwich strucrues under low column buckling loading [13]. The all works focused only on polymer core (honey comb strucrues) but non of the work is focused on different shape and strucures of polymer core for buckling studies.

Moreover, the relation between input paramter and buckling behaivuor is inadequately characterized and not very well understood. Therefore, this study investigated the use of the Taguchi method to optimize factors related to the buckling behavour of polymer sandwich strucurers. The factors considered were type of core (sinewave, square or tringular), thicness of the fiber reinfroced polymer (FRP) layer and loading rate; three conditions of each factor were considered.Taguchi's orthogonal arrays (OA)[14] are highly fractional orthogonal designs. The Taguchi method is a powerful tool for designing high-quality systems based on orthogonal arrays and analysis of variance (ANOVA) to minimize the number of experiments and to effectively improve product quality. This technique can be used to achieve optimal or near-optimal parameters from the selected process parameters. The main objective of the present work was to study the main effects of process parameters on buckling studies using universal testing machine.

II EXPERIMENTAL STUDIES

The corrugated core sandwiches of various thicknesses (0.5mm, 0.75mm, 1mm) and shape (sinusoidal, square, and triangular) were fabricated using epoxy and glass fiber by hand layup technique. The materials used for the preparation of composite laminates are Epoxy resin LY556 (10% amine based hardener), E-Glass Fiber- Plain woven - 0/90 = 200 gsm and Standard Epoxy Adhesive. Edgewise (buckling) compression test is carried out according to ASTM 364 – 99 standard in order to find the compressive properties of the sandwich structure in the direction parallel to the face sheet plane. This test provides a basis for judging the load carrying capacity. The sandwich column, no matter how short, usually is subject to a buckling type of failure unless the facings are so thick that they themselves are in the short column class. The failure of the facings manifests itself by wrinkling of the facing, in which the core deforms to the wavy shape of the facings; by dimpling of the facings into the core; or by bending of the sandwich, resulting in crimping near the ends as a result of shear failure of the core or failure in the facing-to-core bond. Specimens of three types of core geometry and thickness were tested. The dimensions of the specimens are 152.4 mm long, 52 mm width and 15.2 mm thickness; three specimens of each type were tested. The test is done using a UTM of 10 tone capacity manufactured by as shown in Fig. 1.

Fig. 1: Edge wise compression test of a specimen using UTM

Table 1 indicates 9 sets of coded conditions used for forming the design matrix. The method of designing such a matrix has been mentioned in [15]. For the convenience of recording and processing the experimental data, upper and lower levels of the factors were coded as +1 and -1, respectively, and the coded values of any intermediate levels was calculated [16]. The input parameters chosen for the experiments are (a) type of specimens; (b) FRP layer thickness and (c) strain rate in while the response function is maximum buckling load and minimum buckling deformation. In the present analysis, an L9 orthogonal array with three columns and 9 rows is used. This array can handle three level process parameters. The experimental layout for the present work

using the L9 orthogonal array is shown in Table 1. A statistical analysis of variance (ANOVA) is performed to identify the process parameters that are statistically significant. Based on ANOVA the optimal combination of the parameters is predicted.

Table 1: Experimental layout using L9 array with responses

Type of specimen	Skin thickness, mm	Strain rate, mm/min	Buckling strength, N	Buckling deformation, mm
1	0.5	1	614	12.49
1	0.75	2	8075	5.78
1	1	3	10825	4.89
2	0.5	2	2168	7.24
2	0.75	3	4100	5.00
2	1	1	5847	5.13
3	0.5	3	906	7.79
3	0.75	1	1283	5.99
3	1	2	5855	3.65

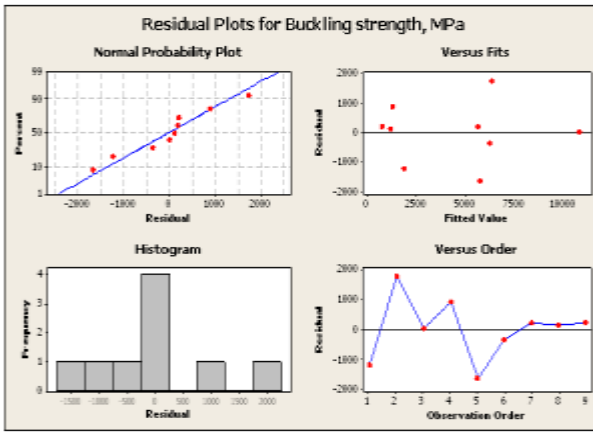
III RESULTS AND DISCUSSION

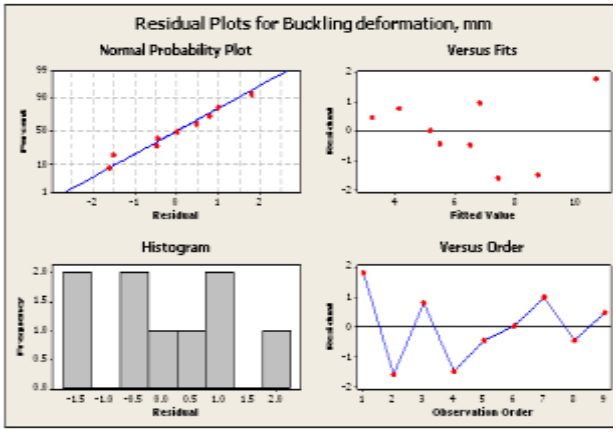
The measured buckling results for all the 9 samples as per typical design matrix are presented in Table 1. To establish the correlation between the buckling parameters such as type of structure, layer thickness and strain rate and responses such as buckling strength and buckling deformation MINITAB multiple linear regression model is used. The regression coefficients of the models are 0.86 and 0.91(R2) respectively.

Buckling strength = -3884.06 - 1911.56 Structure + 12559.5 thickness + 1347.88 strain rate

Max Def= 17.2517 - 0.955 Structure - 9.23333 thickness - 0.988333 strain rate.

Figure 2 indicates scatter plots for a) maximum buckling load, b) maximum buckling deformation of the different sandwich structures and reveals that the actual and predicted values are close to each other within the specified limits.





3.1 Effect of parameters on buckling responses

The above developed statistical model can be employed to predict buckling response and their relationship for the range of parameters used in the investigation by substituting their respective values in the coded form. Based on these models, effects of the process parameters on the buckling responses were computed and plotted, as depicted in Fig. 3 & 4.

a)

b)

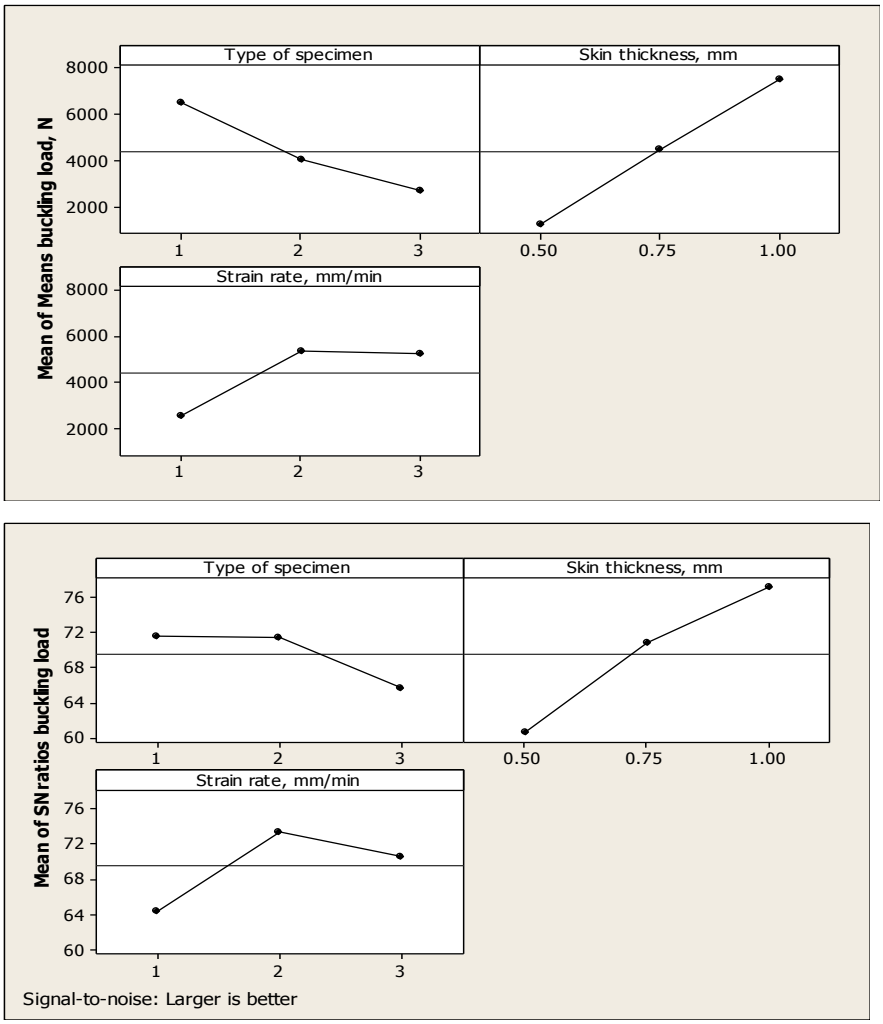


Fig. 3: a) Main and b) S/N ratio parameters of type of specimen, FRP skin thickness and strain rate on buckling strength.

3.1.1 Main effects on buckling strength

Fig. 3(a) shows mean buckling strength as a function of all three parameters. It is seen that for specified conditions, the type of specimen (1) have significant effects that means the sinusoidal specimen shows maximum strength compare to square and triangle. Buckling load response appears to be sensitive to the skin thickness. The buckling strength increases with increase in thickness of the FRP layer almost exponentially. FRP thickness shows maximum buckling deformation strength. Other parameters such as strain rate and type of specimen influenced little on buckling behaviour. Fig. 3(b) shows S/N ratio graphically on the based on larger the better from three repetitive experiments. As per S/N ratio the optimum parameters to obtain buckling

strength are Sine core structure, 1 mm thick skin and 2 mm / min strain rate. This combination gives maximum strength of the structures.

a)

b)

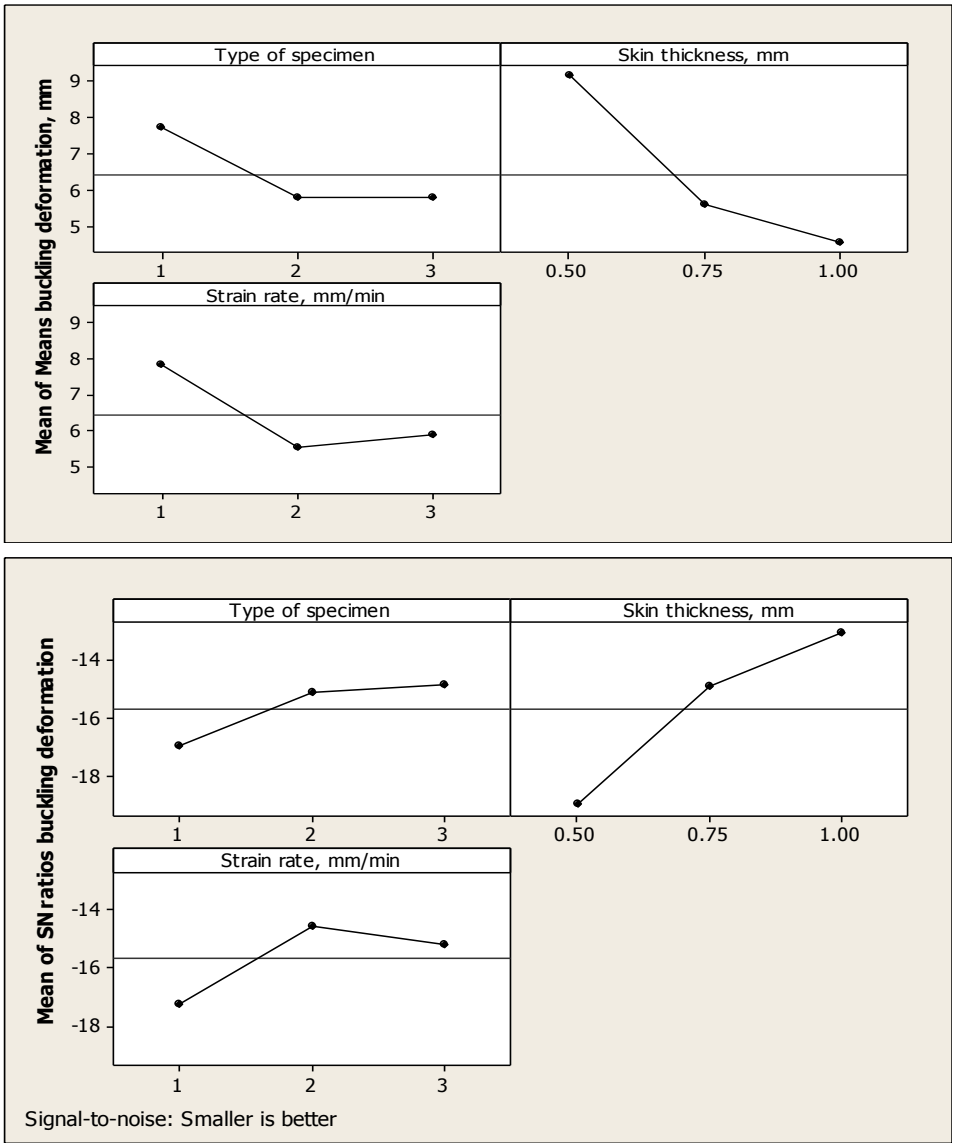


Fig. 4. a) Main and b) S/N ratio parameters of type of specimen, FRP skin thickness and strain rate on bulking behaviour.

3.1.2 Main effects on buckling deflection

Fig. 4(a) shows mean buckling deformation as a function of all three parameters. The buckling deformation resistance is maximum in square and triangular corrugated sandwich structure. The FRP thickness shows maximum buckling deformation resistance. Other parameters such as strain rate and type of specimen influenced little on buckling behaviour.Fig. 4(b) shows S/N ratio graphically on the based on smaller the better from three repetitive experiments. As per S/N ratio the optimum parameters to obtain buckling strength are triangular core structure, 1 mm thick skin and 2 mm / min strain rate. The triangular section are highly rigid member and act as a brittle structure. This combination gives minimum deflection of the structures.

3.2. Interaction effect

3.2.1 Effect of parameters on buckling strength

Fig. 5 shows the combined effect of a) type of specimen vs. skin thickness b) type of specimen vs. strain rate and c) skin thickness vs. strain rate. It is clear from the Fig. 5(a) that the buckling strength increases with increasing skin thickness and sinusoidal has higher buckling strength than other square and triangle specimens. The skin thickness m influences more on buckling strength (it encloses more number of load regions along its axis). Similar observation can be seen for type of specimen vs. strain rate shown in Fig. 5(b). Buckling strength is improved after strain rate varies from 1 to 1.5 mm/min. Fig. 5(c) clearly shows the higher density colour shown at topmost right coroner that shows the influence of skin thickness and strain rate are most influencing parameters on buckling strength. Left bottom most corner lower density colour shows minimum buckling load on the specimen.

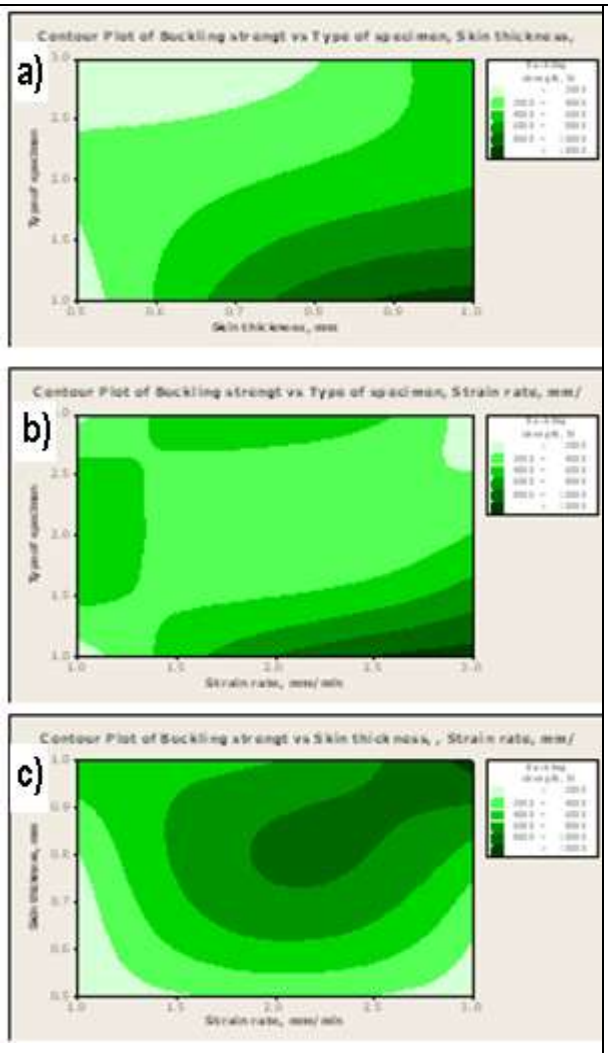


Fig. 5: Contour plot for buckling strength of a) Type of specimen v/s Skin thickness b) Specimen type v/s Strain rate and c) Skin thickness v/s Strain rate.

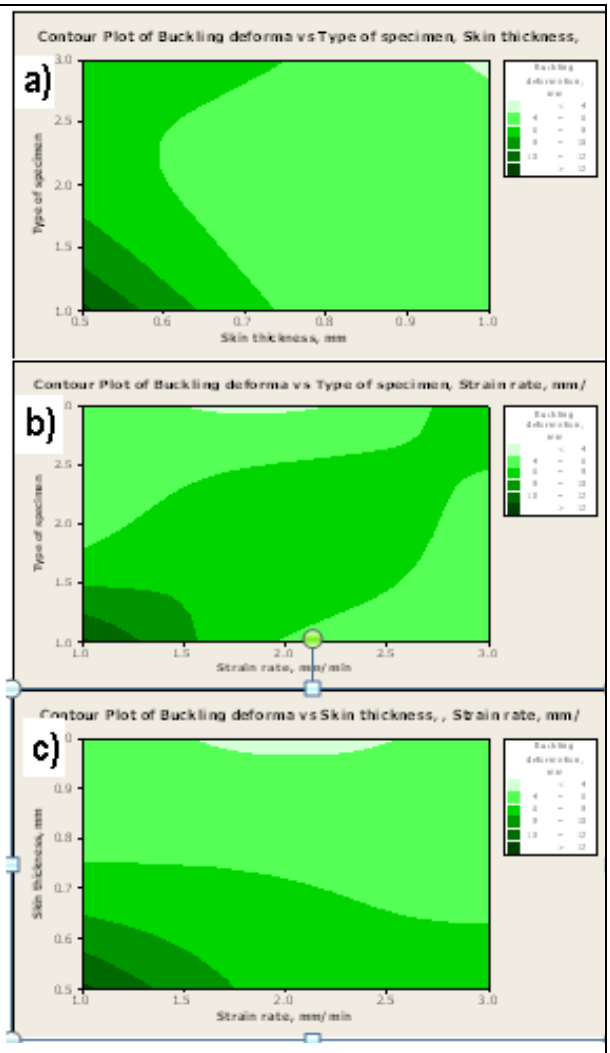


Fig. 6: Contour plot for buckling strength of a) Type of specimen v/s Skin thickness b) Specimen type v/s Strain rate and c) Skin thickness v/s Strain rate.

3.2.3 Effect of parameters on deflection

Fig. 6 shows the combined effect of a) type of specimen vs. skin thickness b) type of specimen vs. strain rate and c) skin thickness height vs. strain rate. Fig. 6 (a) shows effect of type of specimen v/s skin thickness on deflection. The both type of specimen and skin thickness show great influence on the deflection. Higher the skin thickness the lower the deflection and triangular specimen shows lower deflection and Sinusoidal specimen shows higher deflection. Fig. 6(b) shows type of specimen and strain rate influence on deflection of sandwich structures. It is similar to previous graph but it is symmetric about diagonal axis. The strain rate inversely influences on deflection and triangular type corrugation shows least deflection and sinusoidal type corrugation shows maximum deflection. Fig. 6(c) shows skin thickness and strain rate are inversely proportional to buckling deformation. Sinusoidal specimen at strain rate between 1.5 to 2.5 mm/mm produces low bulking deformation.

ANOVA is used to judge whether or not the experimentally found significant factors are statistically significant. The significance can also be judged by calculating F- or P-values. Furthermore, the calculated F-values are compared with the theoretical extreme values for the F distribution. In ANOVA, the meaning of 5% significance level means one in twenty and 1% means one in hundred. This indicates that the parameters falling in 1% significance level is most dominant factor and 5% significance level is the next dominant factor. The factors that are not falling either 1% or 5% are not significant factors. From ANOVA of maximum buckling strength as shown in Table 2, it can be seen that the most dominating factor among the main factors is FRP layer thickness, since it has got higher value of F statistics. The next dominating parameter is the type of specimen and the least effecting factor is strain rate.

Table 2. Analysis of Variance for Buckling load, using Adjusted SS for Tests (buckling strength)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Strucure	02	22539252	22539252	11269626	6.31	0.137
Thickness	02	59180582	59180582	29590291	16.56	0.057
Strain rate	02	15029743	15029743	7514871	4.20	0.192
Error	02	3574284	3574284	1787142		
Total	08	100323861				

From the ANOVA results for buckling deformation absorbing of the sandwich structure given in the Table 3 it can be seen that the most dominating factors among the main factors is the thickness of the skin, next influence factor is strain rate and the least affecting factor is the structure of the specimen.

Table 3. Analysis of Variance for Buckling stress, using Adjusted SS for Tests (buckling deformation)

Source	DF	Seq SS	Adj SS	Adj MS	F	P
Strucure	02	7.3734	7.3734	3.6867	4.31	0.188
Thickness	02	35.2217	35.2217	17.6108	20.57	0.046
Strain rate	02	9.3721	9.3721	4.6860	5.47	0.154
Error	02	1.7123	1.7123	0.8561		
Total	08	53.6794				

IV CONCLUSION

The buckling of sandwich structures are investigated by subjecting to axially compressive loading along the axis. The buckling behaviour of polymer sandwich structure is significantly improved by the presence of a corrugated sandwich core due to increase its toughness. However, sandwich structures exhibit different strength depending on the types of core geometry used. The optimal parameters combination happens to be type of structure of F value 6.31, FRP layer thickness 16.56 and strain rate 4.2, F values indicates FRP layer thickness contributed much higher than that of other parameters. Control factor combination is sinusoidal shaped core, 1 mm thickness of the FRP layer and 2 mm/min strain rate. The sandwich strength increases with increase in thickness of the FRP but the weight also increased. The residual errors associated with the ANOVA are observed to be lower for the factors and the coefficient of regression obtained with the multiple regression values show that the satisfactory correlation is obtained (R^2) .

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